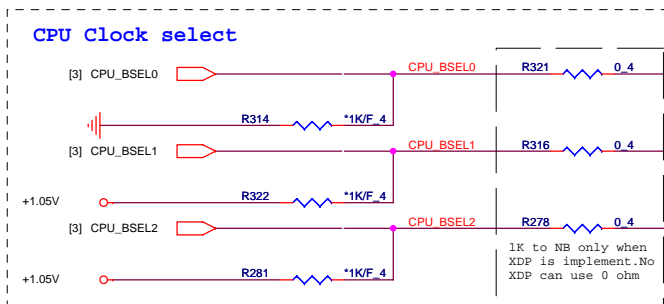
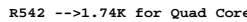


Timing diagram for EMI showing clock signals for various components:

- C501: *33P/50V 4 PCLK KBC
- C503: *27P/50V 4 PCLK ICH
- C495: *33P/50V 4 PCLK_DEBUG
- C518: *10P/50V 4 CLK 48M USB
- C514: *10P/50V 4 CLK 48M CR
- C506: *33P/50V 4 CLK 14M ICH

for EMI



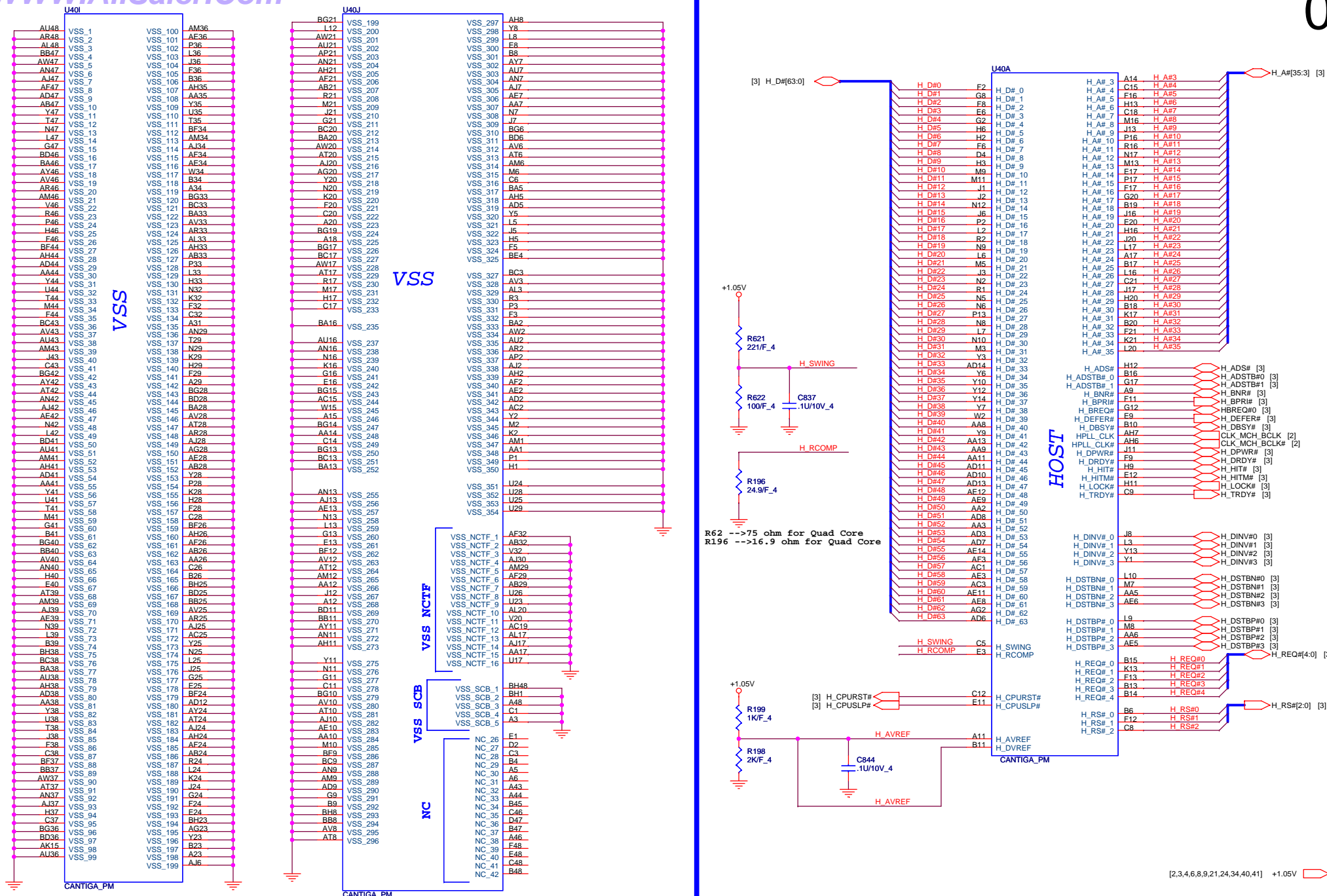


Don't install for DC Change to +5V



Size Custom	Document Number Penryn 1/2	Rev 2B
Date: Tuesday, February 26, 2008		Sheet 3 of 44





MCH_CFG_5 DMIx2 selection
Low = DMI X2
High = DMI X4 (Default)
MCH_CFG_16 FSB Dynamic ODT
Low = Dynamic ODT disabled
High = Dynamic ODT enabled (default)
MCH_CFG_9 PCI Express Graphic Lane
Low: Reverse Lane
High: Normal operation(Default)
MCH_CFG_19 DMI Lane Reversal
Low = Normal operation (Default)
High = Reverse Lanes
MCH_CFG_6 ITPM Host Interface
Low = The ITPM Host Interface is enabled2
High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel(R) Management Engine Crypto
Low: Intel(R) Management Engine Crypto
High: Intel(R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel(R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)
MCH_CFG_10 PCIe Lookback Enable
Low = Enabled3
High: Disabled (Default)
MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating
MCH_CFG_13 MCH_CFG_12 Configuration

0 0 Reserved
1 0 XOR Mode enabled
0 1 All-Z Mode enabled
1 1 Normal operation (Default)

MCH_CFG_20
Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIE
Low = Only digital display port (SDVO/DP/HDMI) or PCIE is operational (default)
High = Digital display port (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port

MCH_CFG_20
000 = FSB1066
010 = FSB800
011 = FSB667
Others = Reserved

[2] MCH_BSEL0
[2] MCH_BSEL1
[2] MCH_BSEL2

TP29 MCH_CFG_3
TP23 MCH_CFG_4
TP64 MCH_CFG_5
TP20 MCH_CFG_6
TP22 MCH_CFG_7
TP24 MCH_CFG_8
TP12 MCH_CFG_9
TP18 MCH_CFG_10
TP14 MCH_CFG_11
TP16 MCH_CFG_12
TP10 MCH_CFG_13
TP12 MCH_CFG_14
TP14 MCH_CFG_15
TP16 MCH_CFG_16
TP18 MCH_CFG_17
TP20 MCH_CFG_18
TP22 MCH_CFG_19
TP24 MCH_CFG_20

[23] PM_SYNC#
[3,21,41] H_DPRSTP#
[10,11] PM_EXTTS#0
[11] PM_EXTTS#1
[23,41] DELAY_VR_PWROGOOD
[12,22] PLT_RST-R#
[3,21] PM_THRMTrip#
[23,41] DPRSLPVR

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[23,41] DPRSLPVR

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[3,21] PM_THRMTrip#
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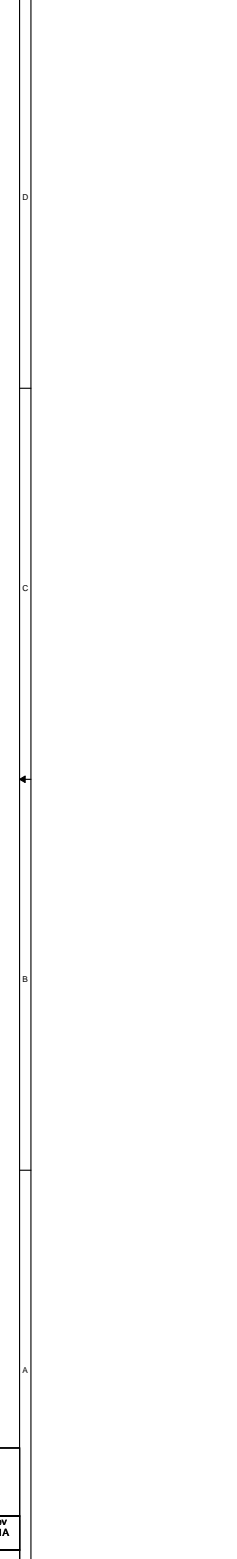
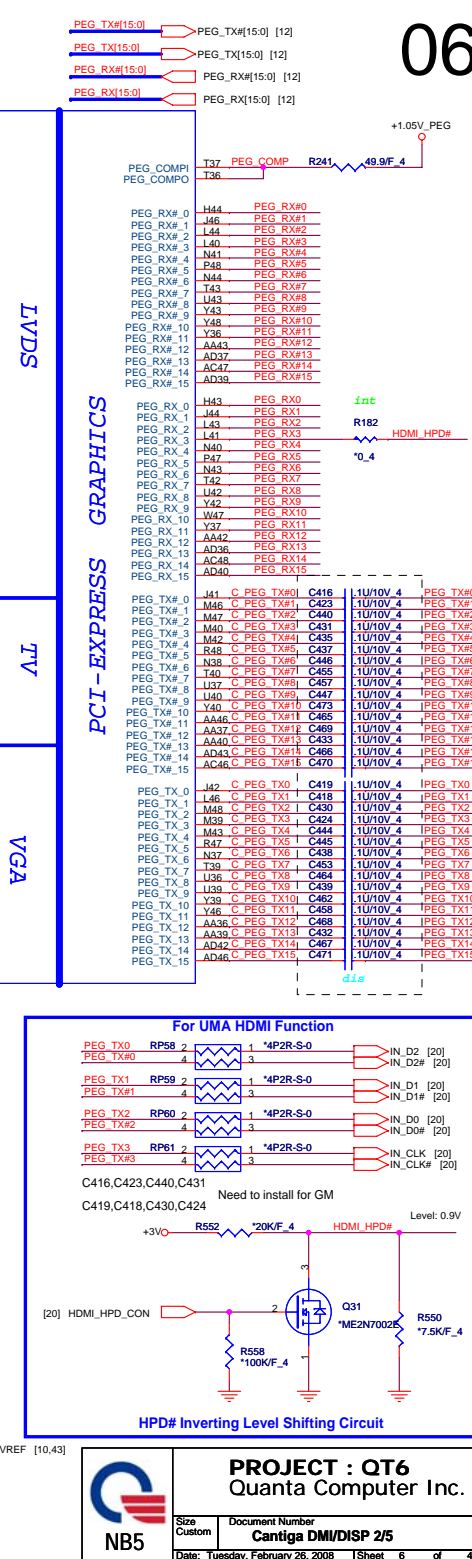
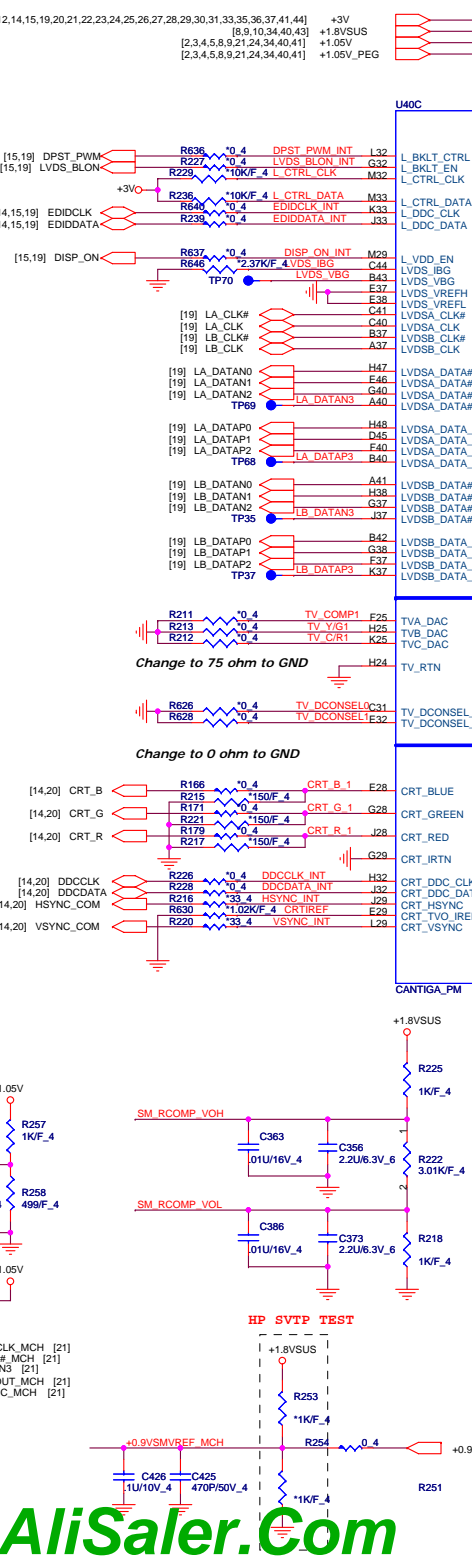
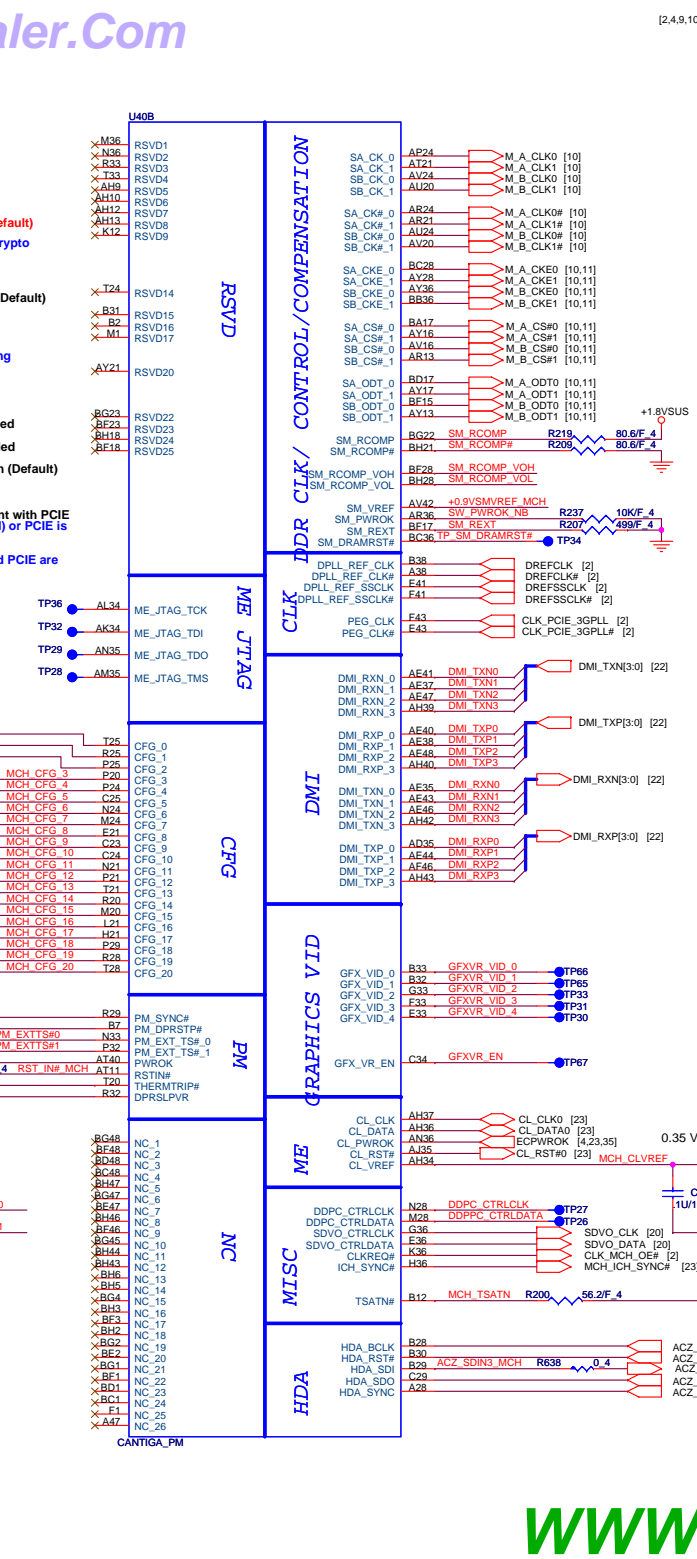
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[23,41] DPRSLPVR

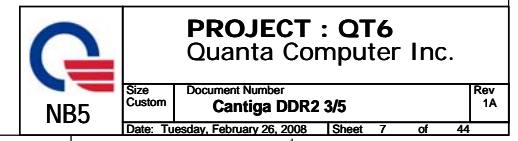
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[11] PM_EXTTS#1
[23,41] DELAY_VR_PWROGOOD
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[3,21] PM_THRMTrip#
[23,41] DPRSLPVR

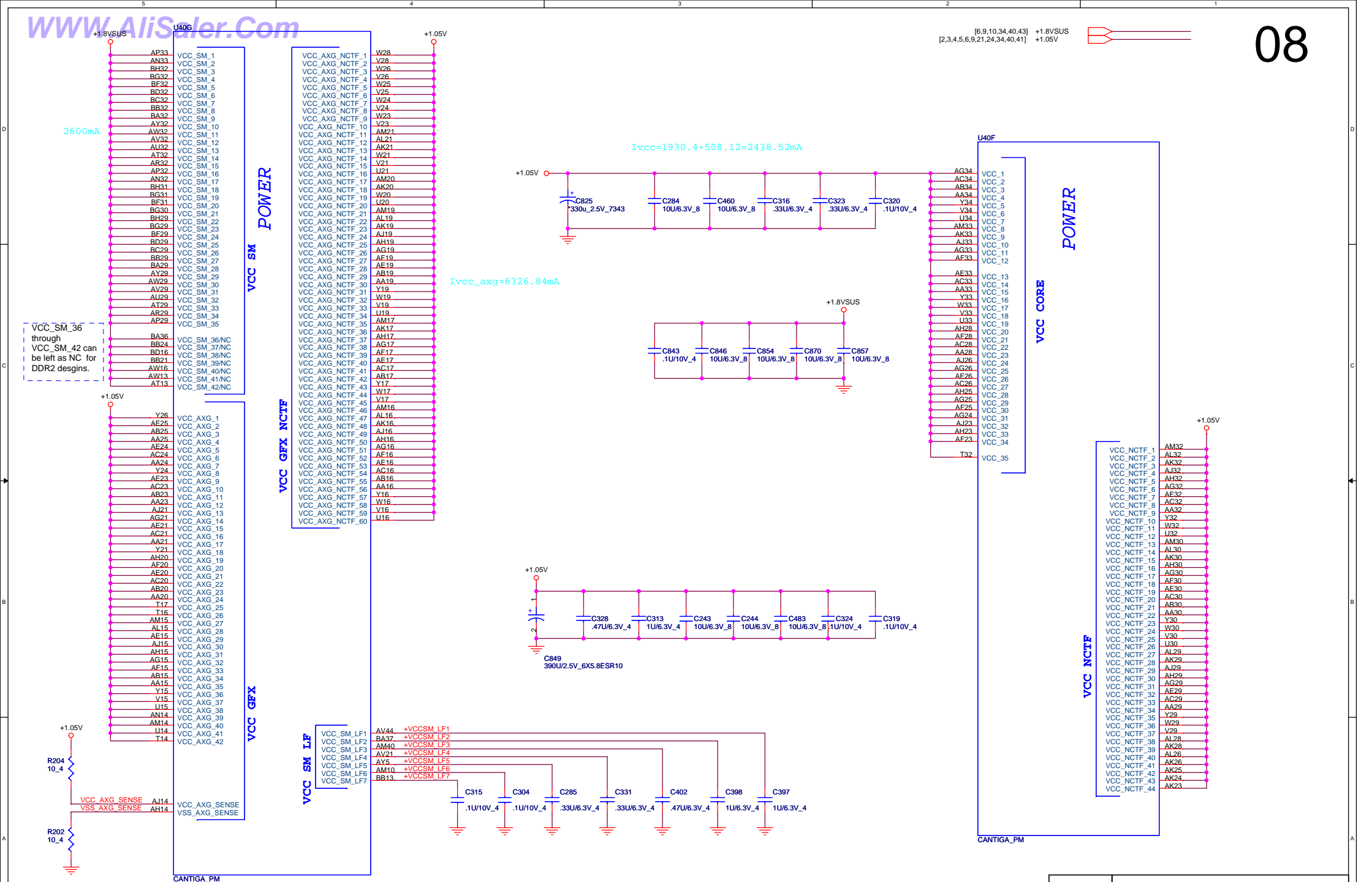
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[11] PM_EXTTS#1
[23,41] DELAY_VR_PWROGOOD
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[3,21] PM_THRMTrip#
[23,41] DPRSLPVR

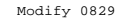
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[3,21,41] H_DPRSTP#
[10,11] PM_EXTTS#0
[11] PM_EXTTS#1
[23,41] DELAY_VR_PWROGOOD
[12,22] PLT_RST-R#
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[23,41] DPRSLPVR



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[12,22] PLT_RST-R#
[3,21] PM_THRMTrip#
[23,41] DPRSLPVR



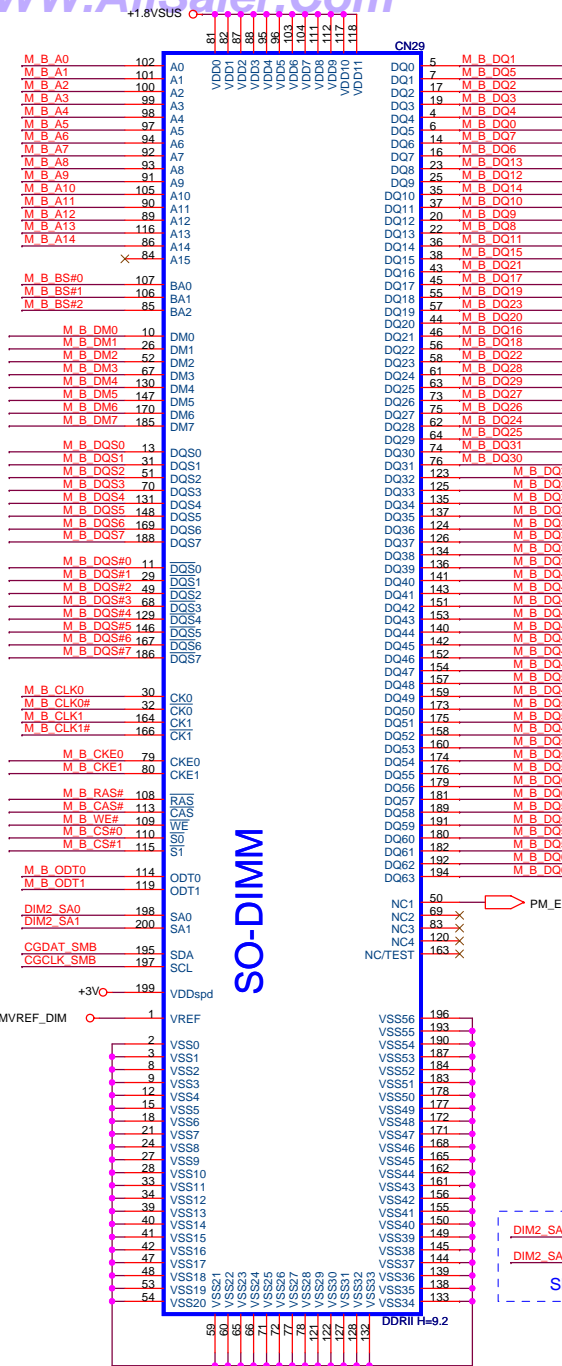






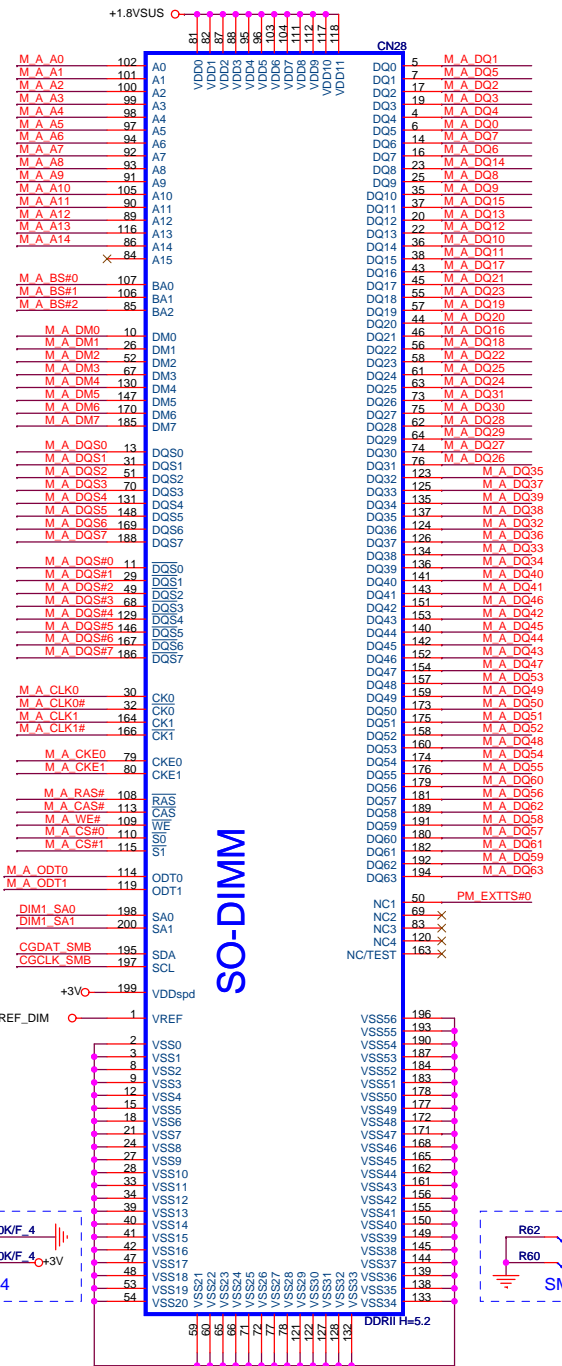
SI-2   /

Modify to U40#AF1 power to +1.05V_MPLL as CRB change



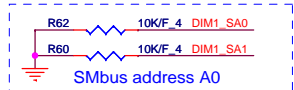
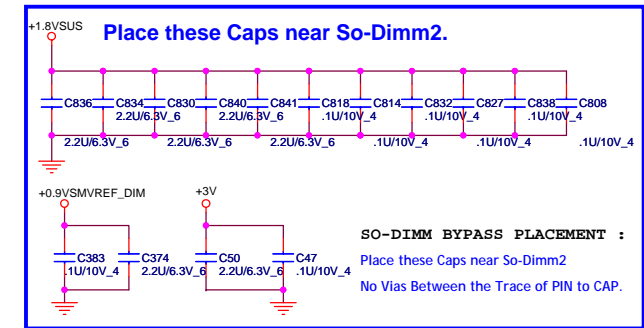
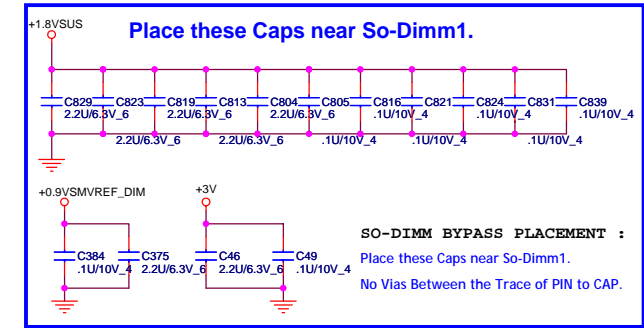
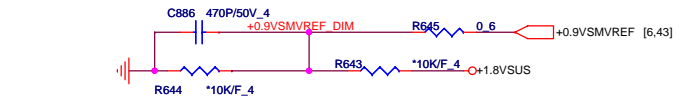
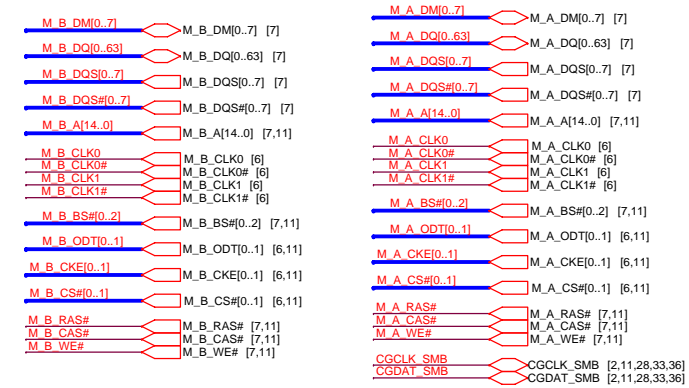
SO-DIMM

H 9.2
DGMK0000036



SO-DIMM

H 5.2
DGMK0000031

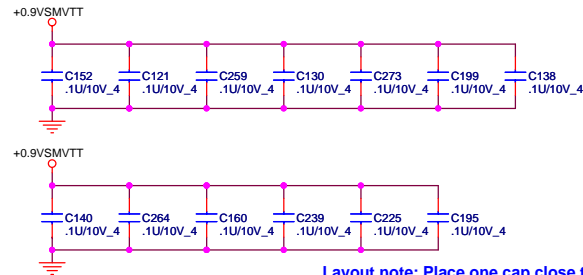


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Quanta Computer Inc.

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	DDR2 DIMM	
Date: Tuesday, February 26, 2008	Sheet 10 of 44	

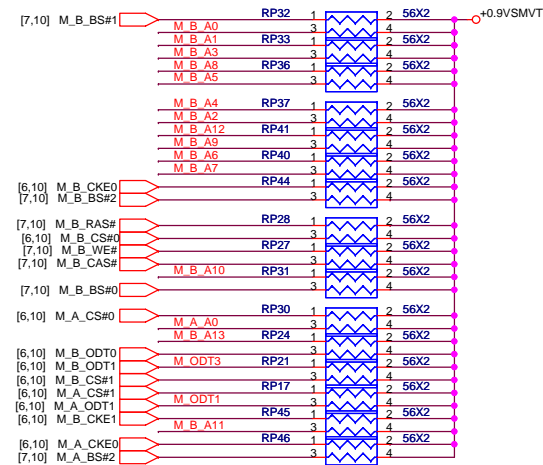
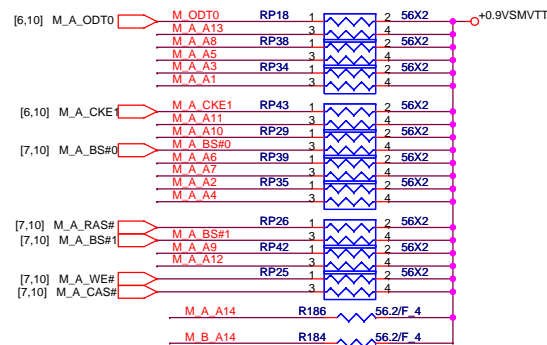
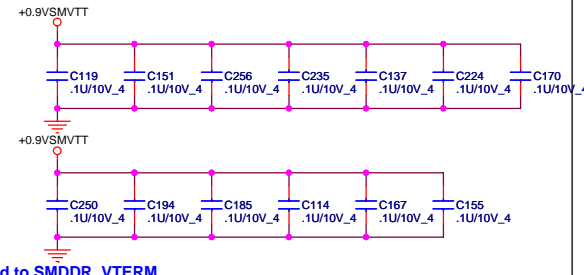
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

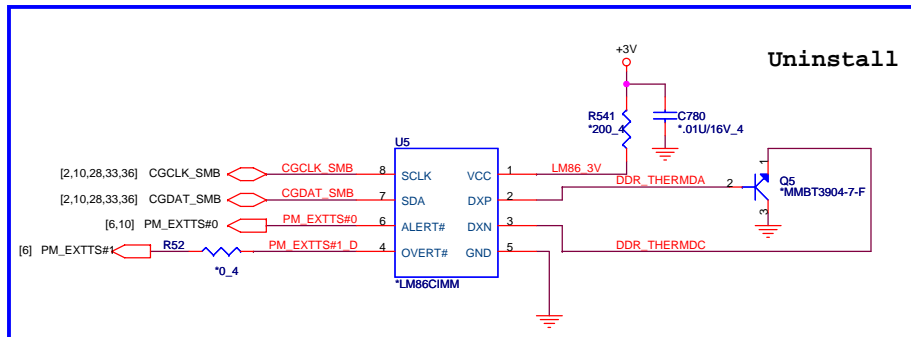


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDR_VTERM

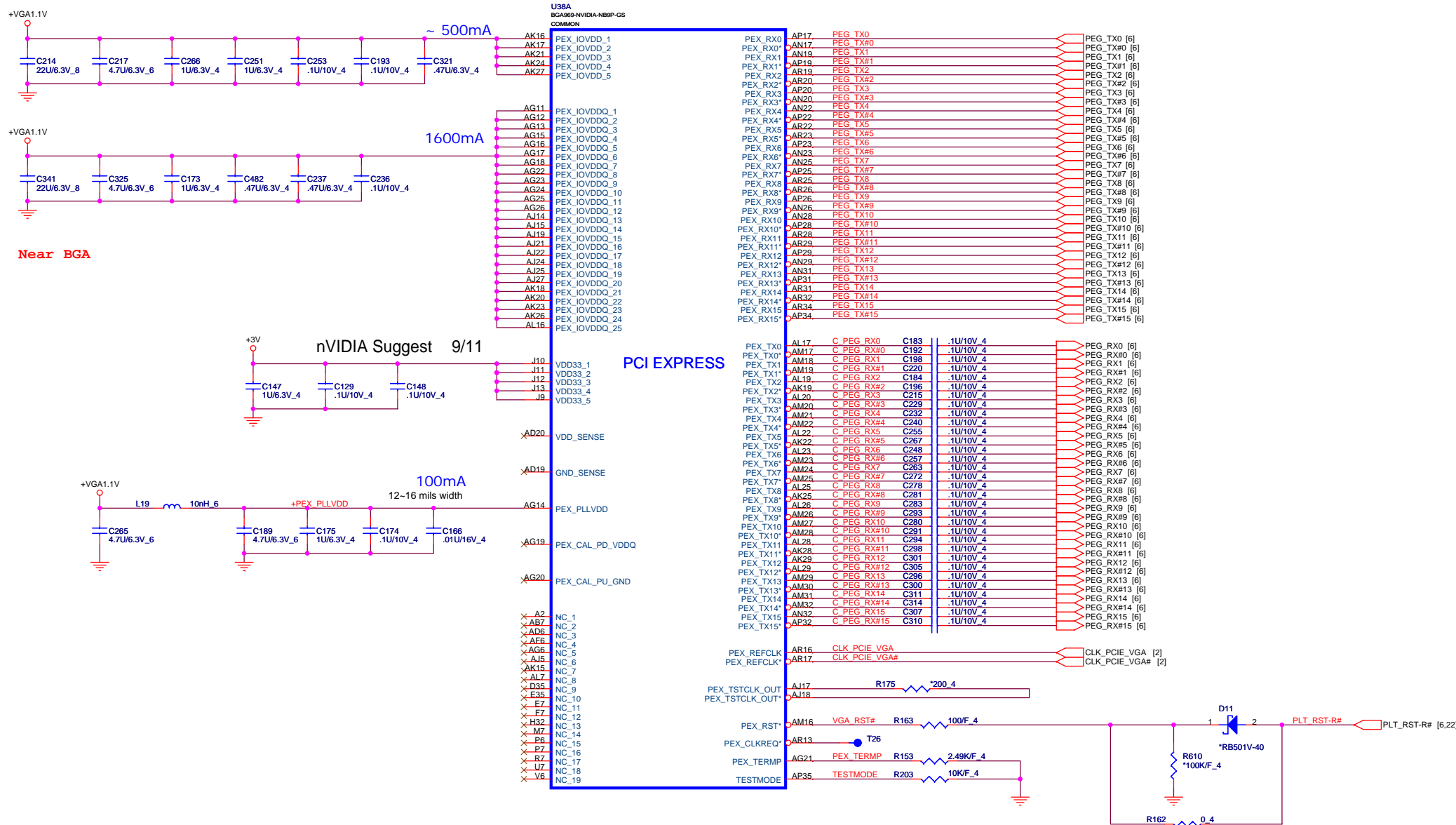
DDRII B CHANNEL

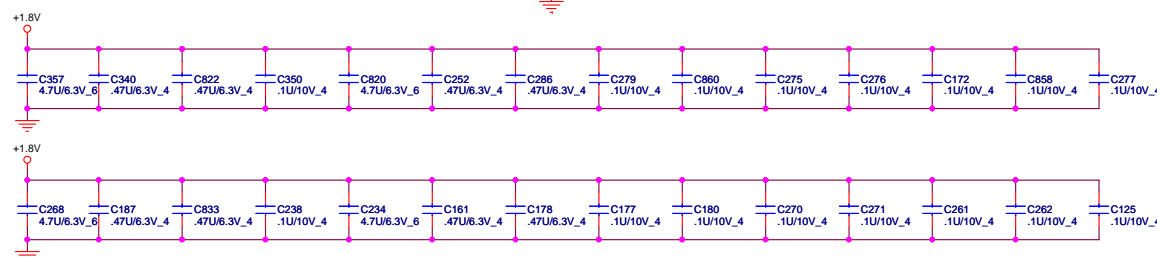
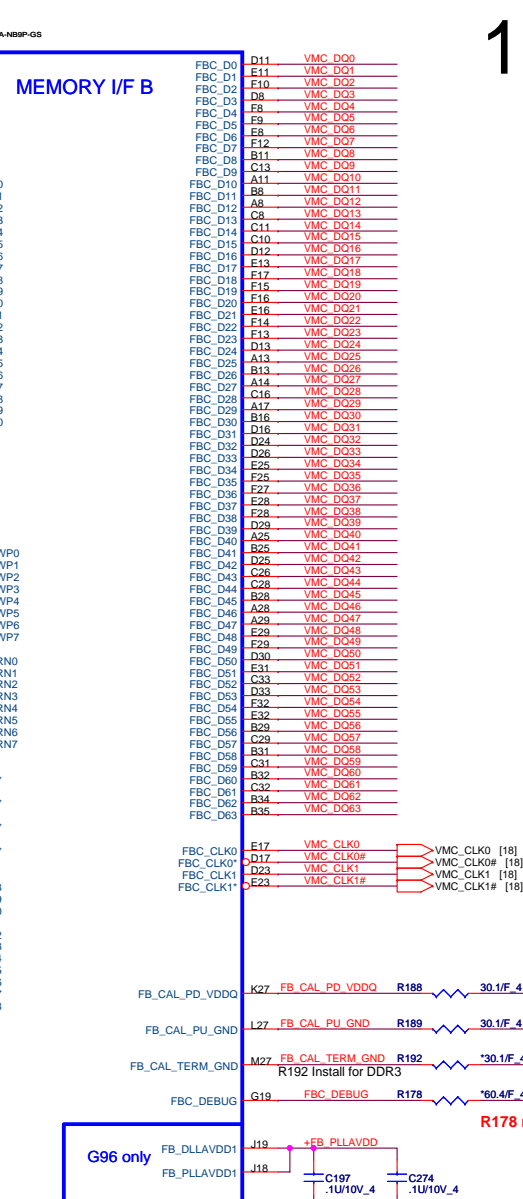
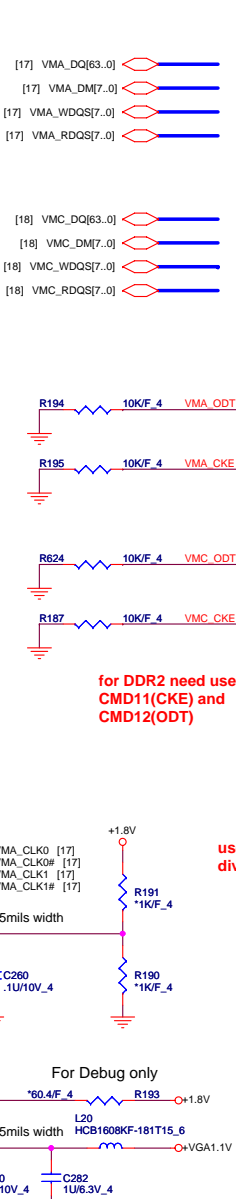
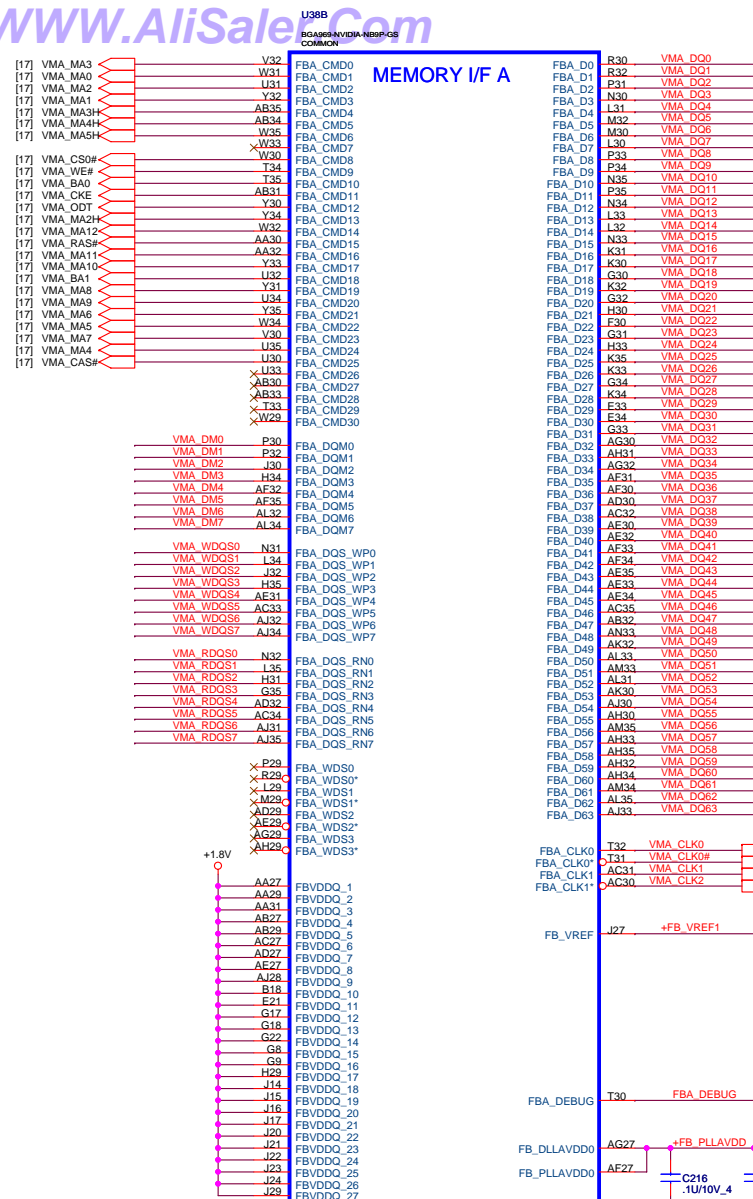


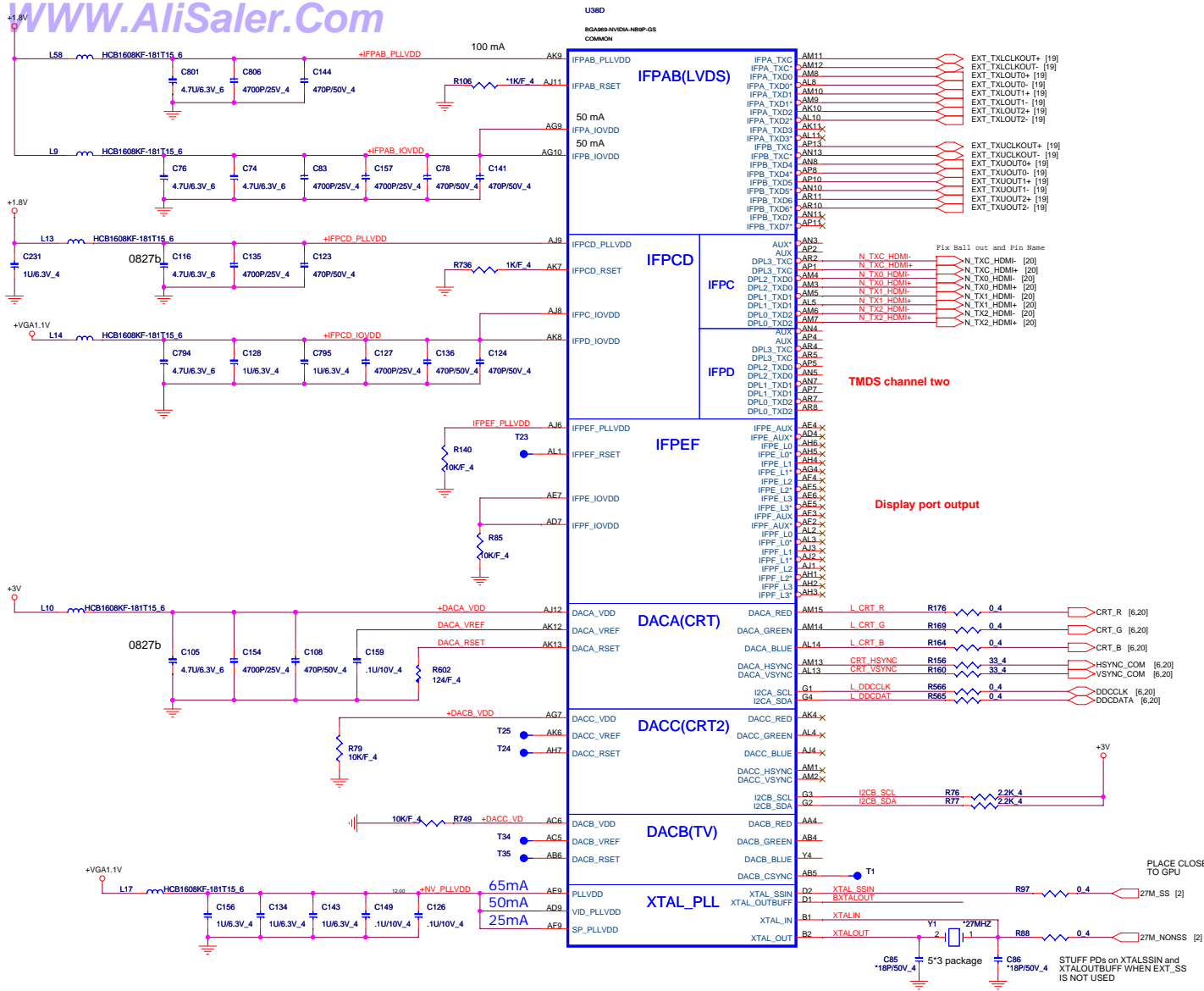
M_B_A[14..0] M_B_A[14..0] [7..10]
M_A_A[14..0] M_A_A[14..0] [7..10]



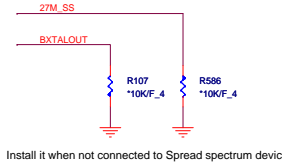
+0.9VSMVTT [43]
+3V [2,4,6,9,10,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,33,35,36,37,41,44]



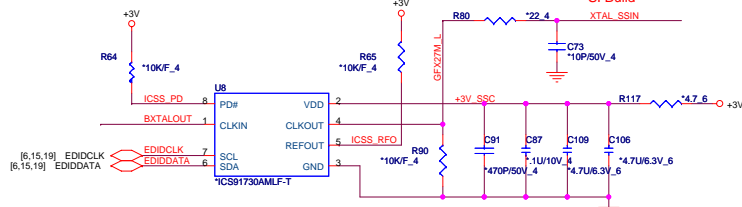




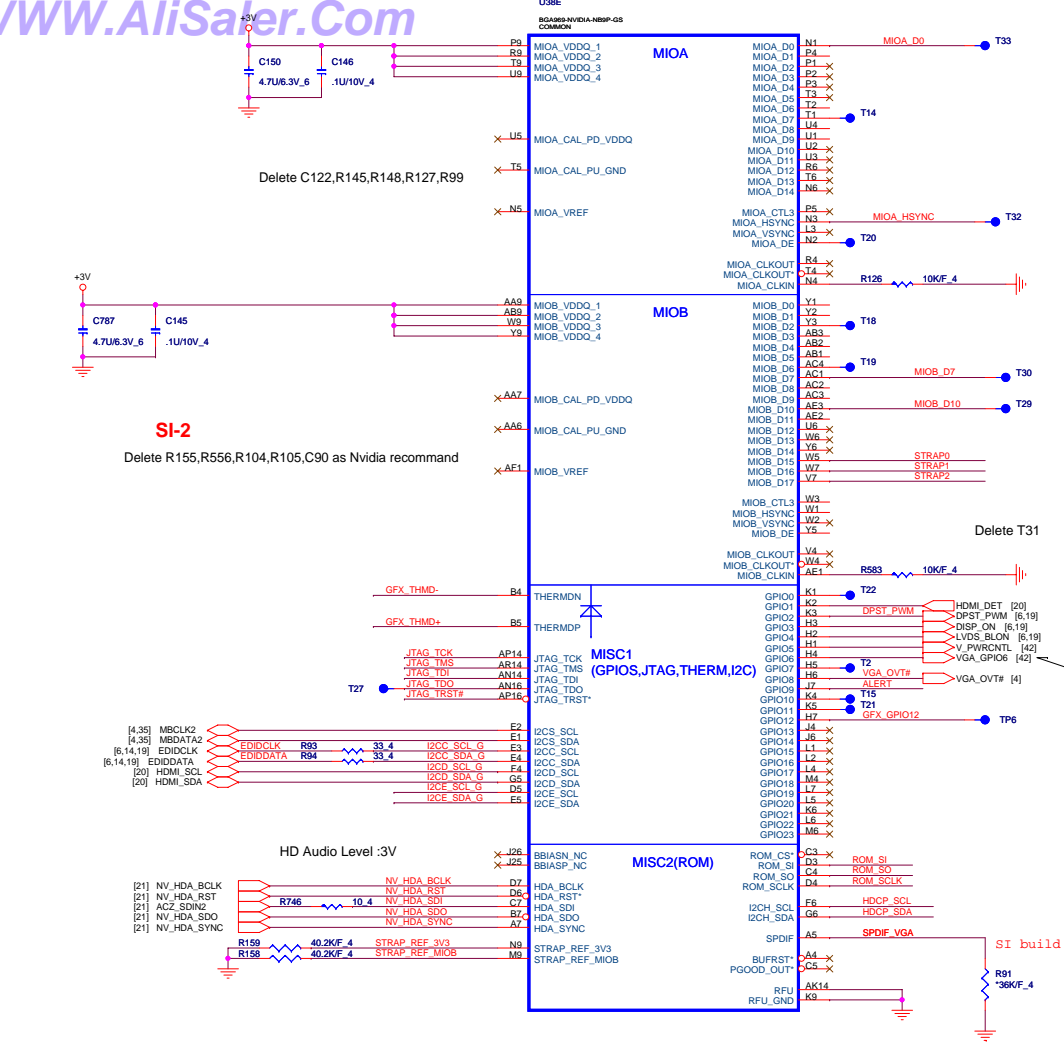
PLACE CLOSE TO GPU



SPREAD SPECTRUM

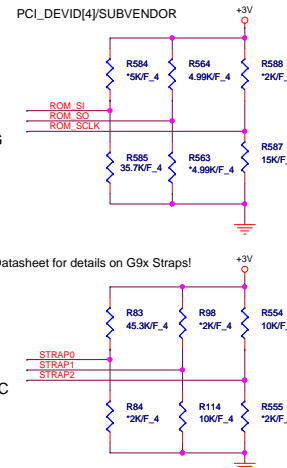


I2C ADDRESS: 0xD4H



NB9P-GS (G96) Straps NB9M-GE (G98) Straps GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



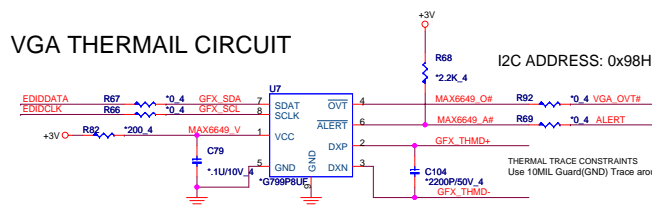
Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP1	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP0	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
	USER[3]	USER[2]	USER[1]	USER[0]

1000
0010
XXXX
XXXX
0001
1111

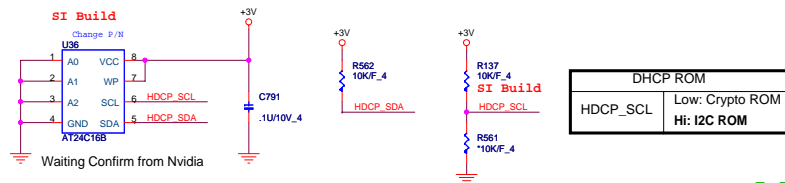
VGA THERMAIL CIRCUIT



NB9X VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
0110	DDR2 32Mx16x8, 128bit, 512MB	Qimonda
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
other	Reserved	

HDCP ROM



PCI_DEVID: STRAP2 R554

NB9M-GE 0x06E 8 1000 PU 5K
NB9M-GS 0x06E 9 1001 PU 10K
NB9P-GE2 0x064 8 1000 PU 5K
NB9P-GS 0x064 9 1001 PU 10K

CS33572FB13 RES CHIP 35.7K 1/16W +-1% (0402)
CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

RAM ID: ROM_SI R585

SAM 0101 PD 30.1K

QIM 0110 PD 35.7K

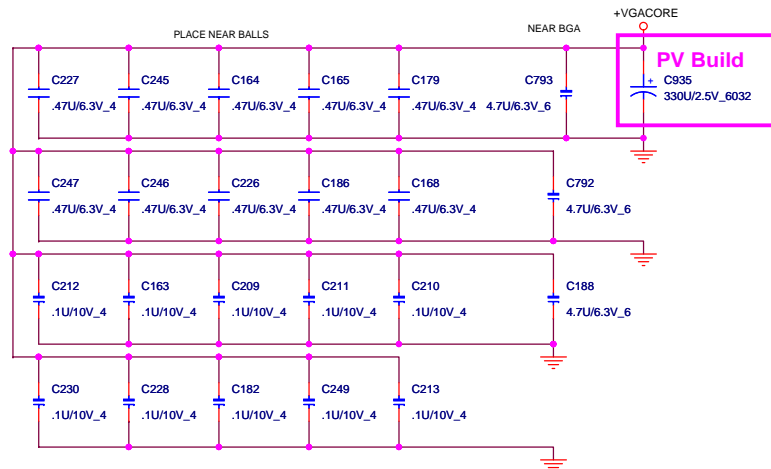
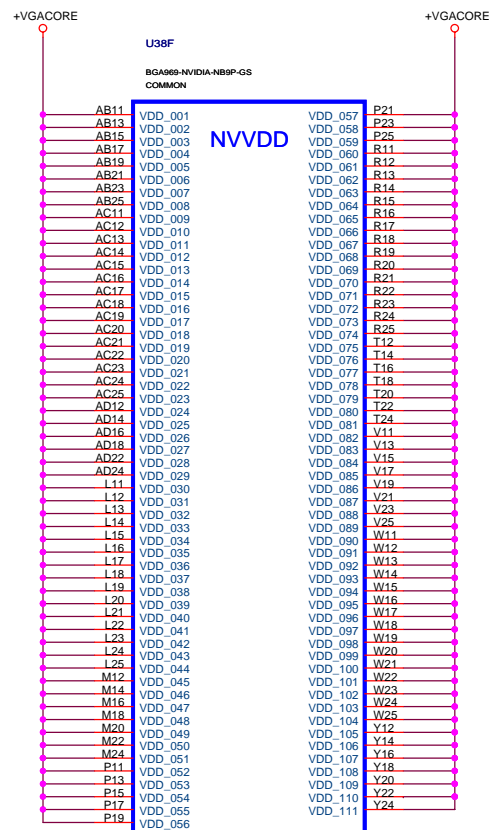
HYN 0111 PD 45.3K



PROJECT : QT6
Quanta Computer Inc.

Size	Document Number	Rev
C	NV9X (GPIO & STRAPS) 4/5	28
Date: Tuesday, February 26, 2008	Sheet 15 of 44	

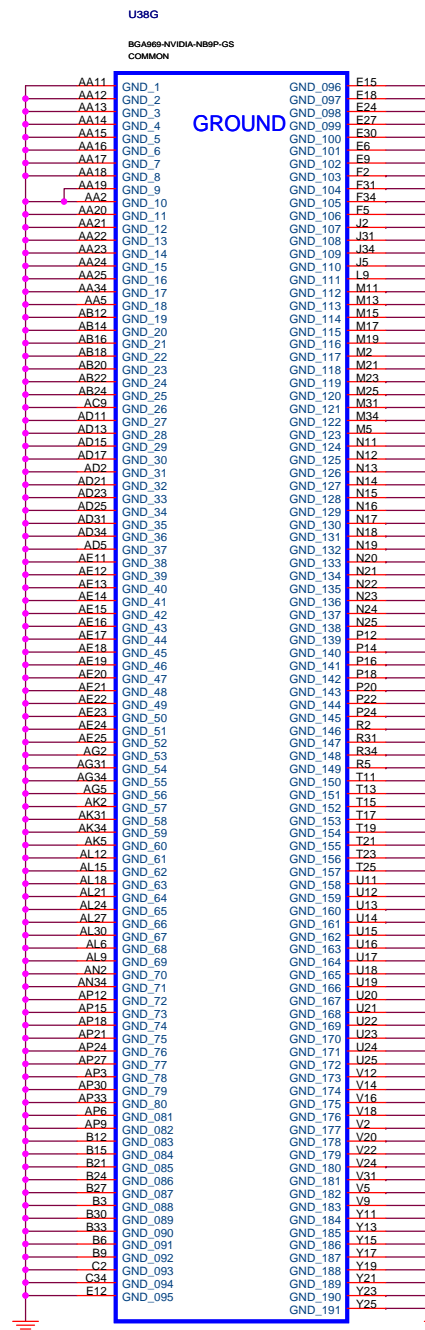
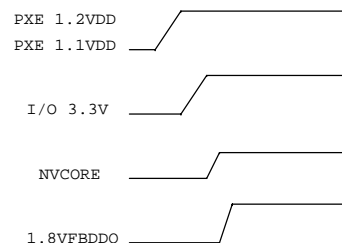
NVVDD Decoupling

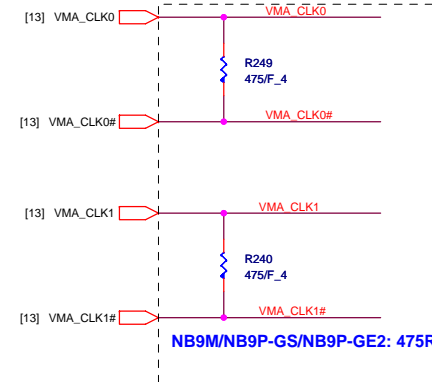


Follow Design Guide DG-03276-001 4.7uFx3 and 0.47x10 uF instead of 0.1uF x10

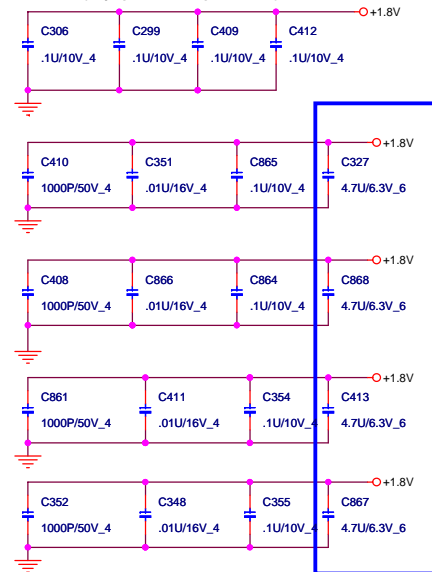
NB9M: VGACORE +0.90V (Normal) , +1.09V



power up sequence











(By pass capacitor)



[13] VMA_DQ[63..0]  

[13] VMA_DM[7..0]  

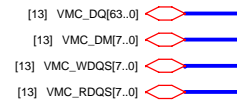
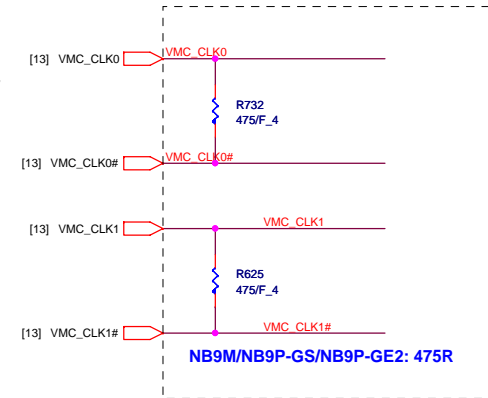
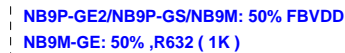
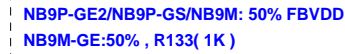
[13] VMA_WDQS[7..0]  

[13] VMA_RDQS[7..0]  

VMA		U42		VREF		J2		VMREFA1	
VMA D057	B9	UD07							15mil
VMA D062	R1	UD08							
VMA D060	D9	UD05							
VMA D061	D1	UD04							
VMA D063	D3	UD03							
VMA D059	D7	UD02							
VMA D056	C2	UD01							
VMA D058	C8	UD07							
VMA D053	F9	LD07							
VMA D052	F1	LD06							
VMA D054	H8	LD05							
VMA D048	H1	LD04							
VMA D050	H3	LD03							
VMA D049	H7	LD02							
VMA D051	G2	LD01							
VMA D055	G8	LD00							
VMA D057	B3	UDM							
VMA D06	F3	LDM							
VMA WD057	B7	UD05							
VMA RDQ57	A8	UD05							
VMA WDQ58	F7	UD05							
VMA RDQ56	E8	LD05							
VMA CLK1	J8								
VMA CLK1#	K8	CK							
VMA BA1	L3	BA1							
VMA BA0	L2	BA0							
VMA MA12	R2	A12							
VMA MA11	P7	A11							
VMA MA10	M2	A10							
VMA MA9	P3	A9							
VMA MA8	P8	A8							
VMA MA7	P2	A7							
VMA MA6	N7	A6							
VMA MA5H	N3	A5							
VMA MA4H	N8	A4							
VMA MA3H	N2	A3							
VMA MA2H	M7	A2							
VMA MA1	M3	A1							
VMA MA0	M8	A0							
VMA ODT	K9	ODT							
VMA CKE	K2	CKE							
VMA CS0#	L8	CS							
VMA WEF#	K3	WE							
VMA RAS#	L7	RAS							
VMA CAS#	K7	CAS							

PROJECT : QT6
Quanta Computer Inc.

Size Custom	Document Number NV9X VRAM-1(GDDR2 BGA84)	Rev 1A
Date: Tuesday, February 26, 2008		Sheet 17 of 44

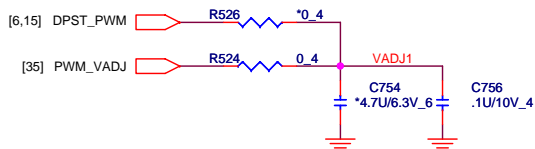
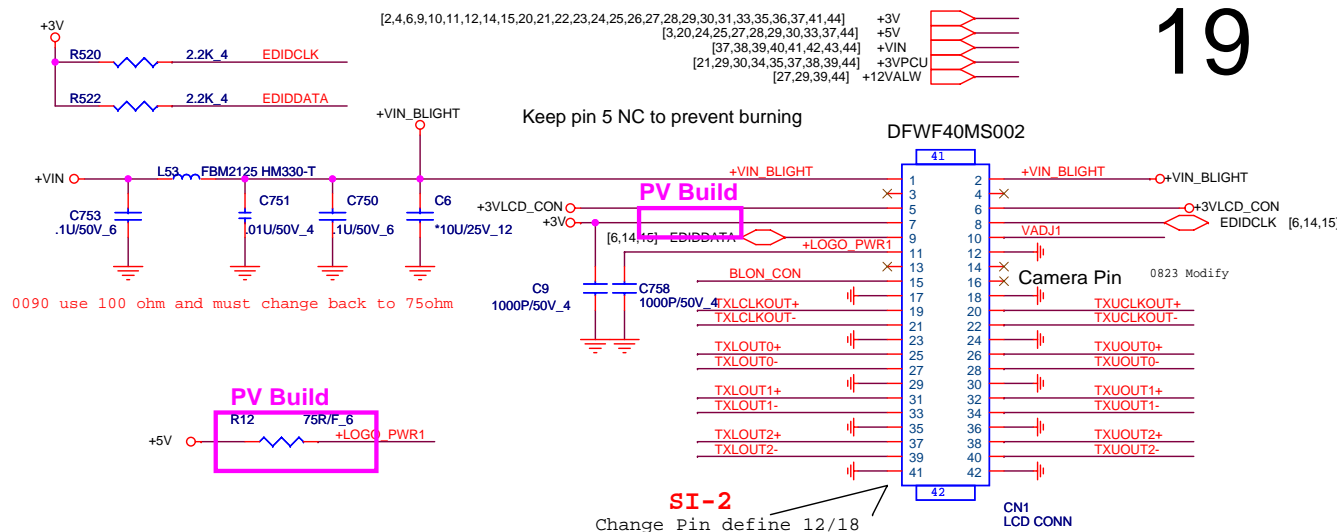


- | | | | |
|---|-------------|--|---------|
| 3 | AKD5FG-T501 | IC SDRAM(84P) K4N51163QG-HC25(FBGA) | Samsung |
| 2 | AKD5FG-T*03 | IC SDRAM(84P)HYB18T512161B2F-25(TFBGA) | Qimonda |
| 1 | AKD5FG-TW31 | IC SDRAM(84P) HY5PS121621CFP-25(FBGA) | Hynix |



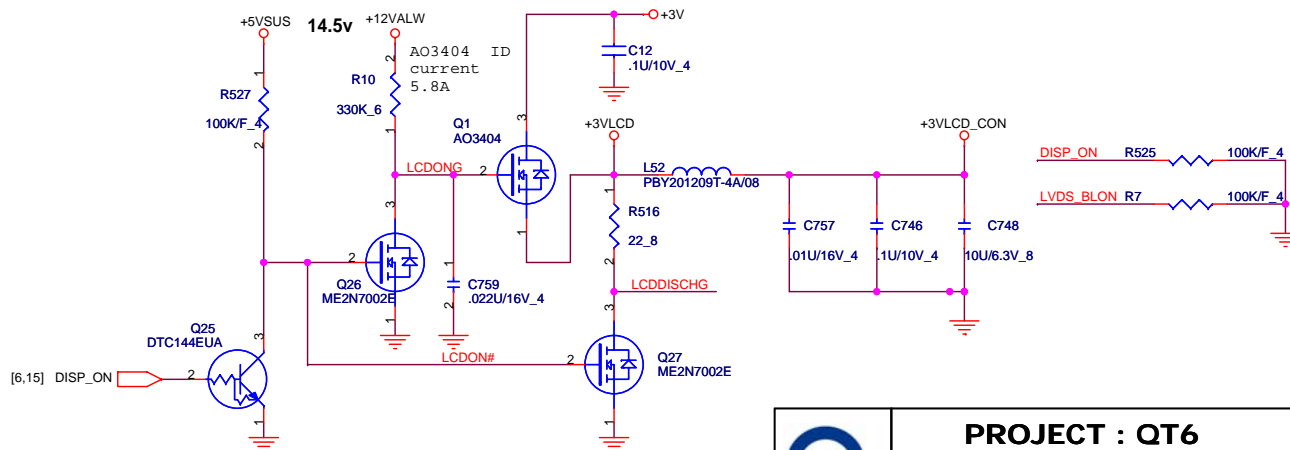
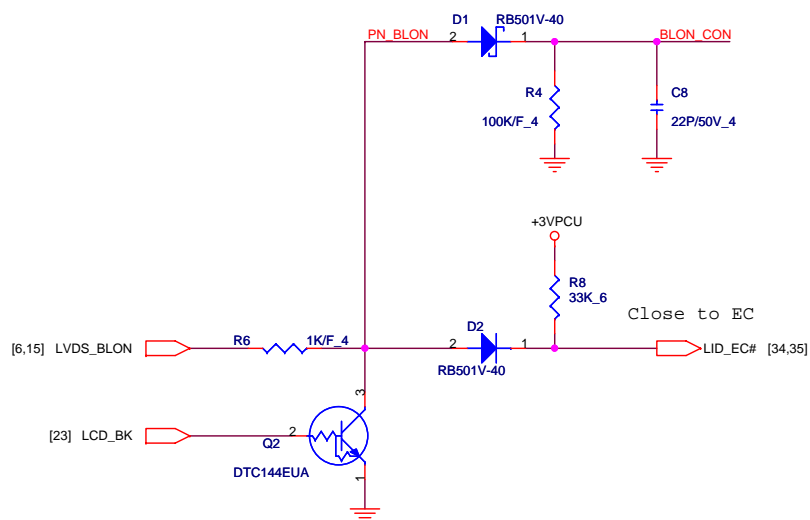
Size Custom	Document Number NV9X VRAM-2(GDDR2 BGA84)	Rev 1A
Date: Tuesday, February 26, 2008		Sheet 18 of 44

OPTION SIGNAL FROM NB FOR UMA VGA



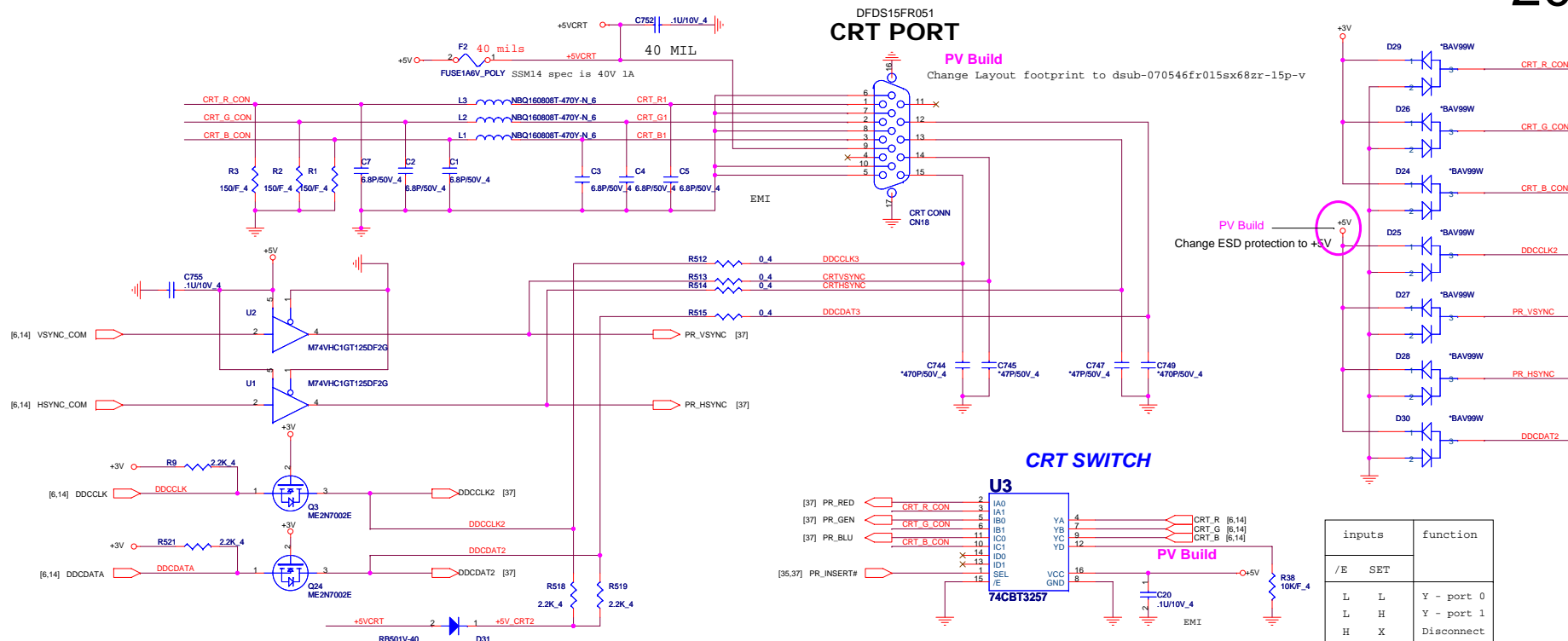
PV Build

Delete CN20,R63,C761(Remove Logo light2)

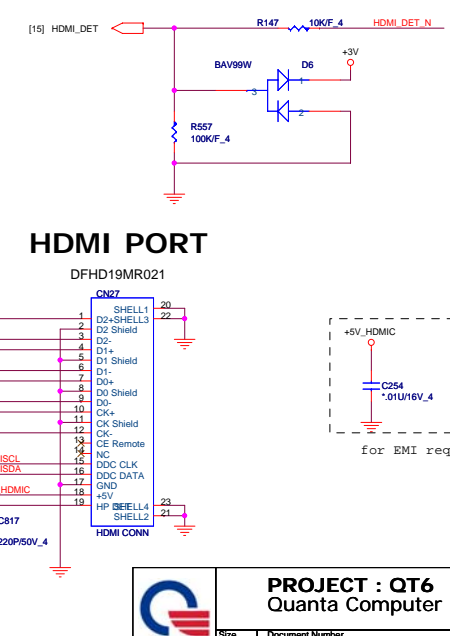
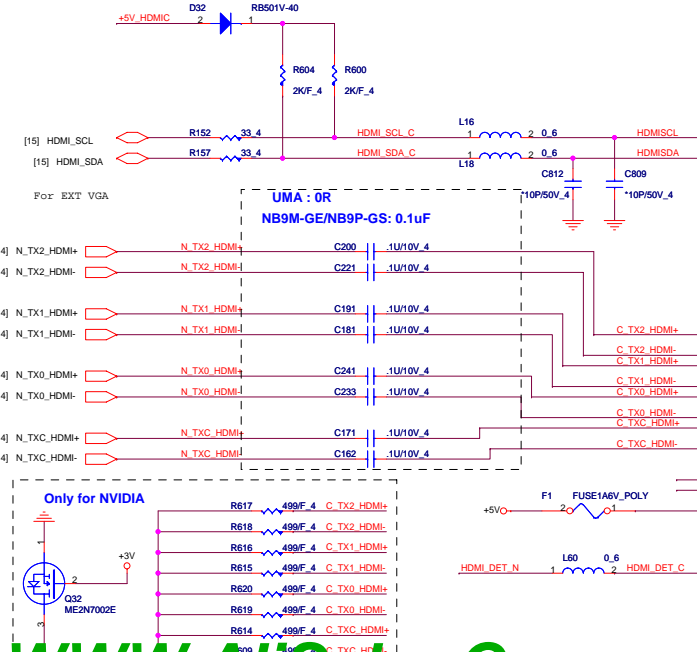
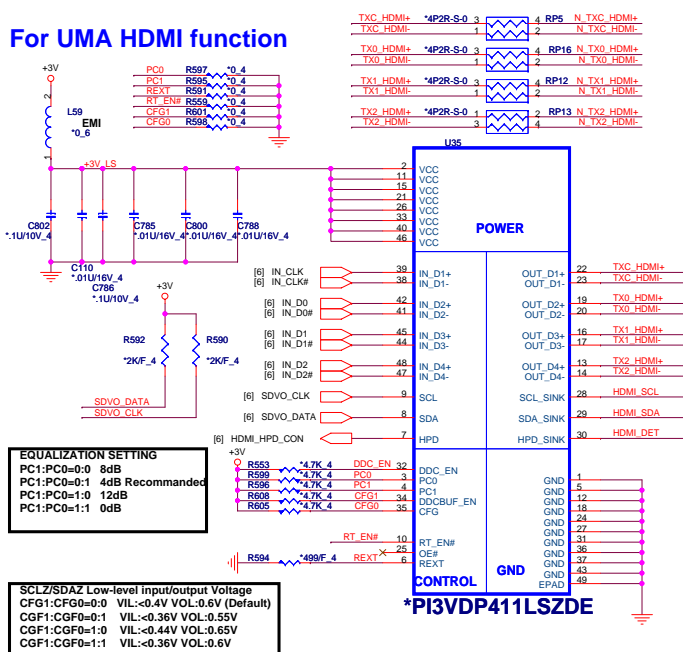


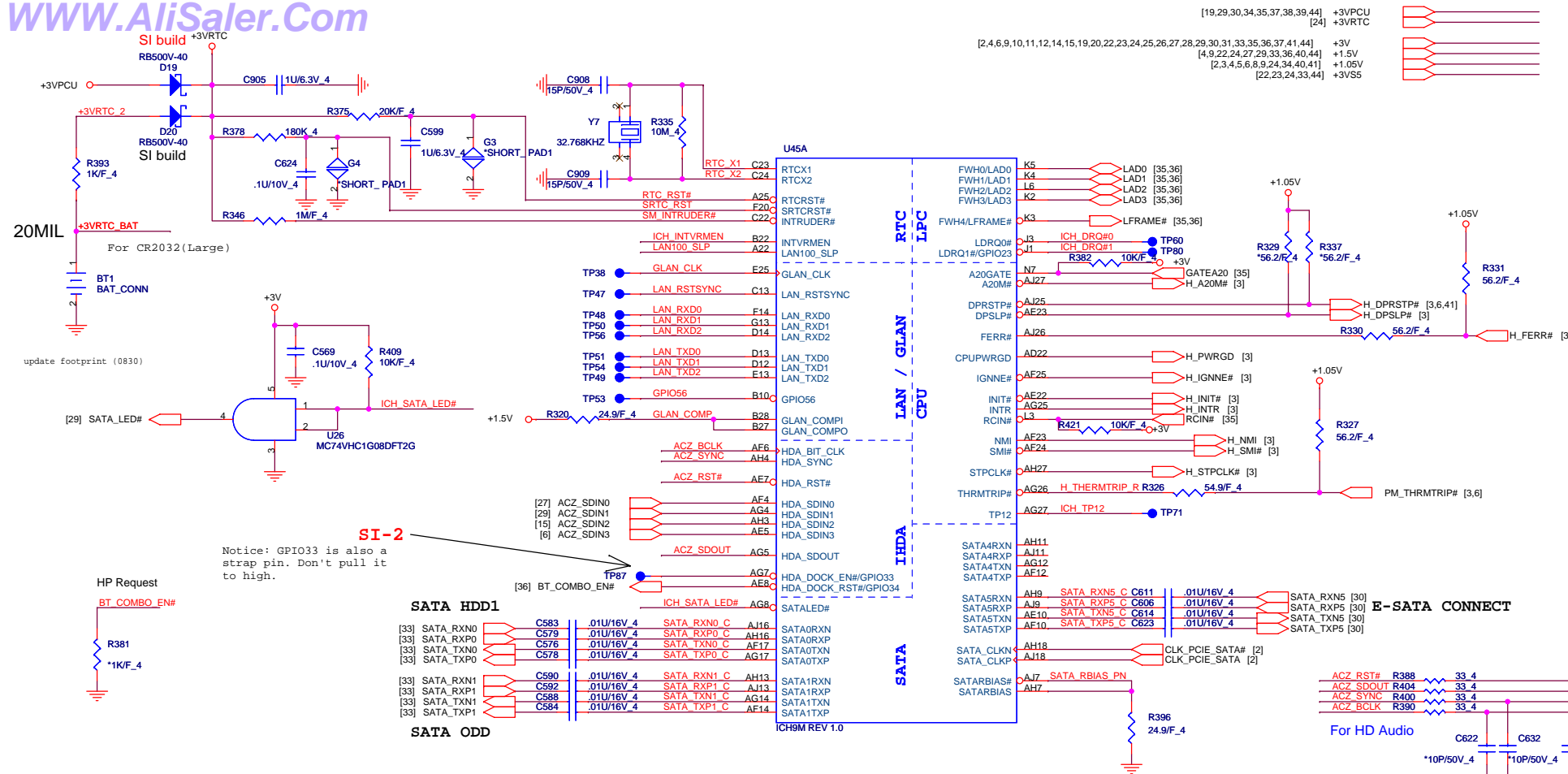
PROJECT : QT6
Quanta Computer Inc.

Size B	Document Number LCD CONN/Lid function
Date: Tuesday, February 26, 2008	Sheet 19 of 44



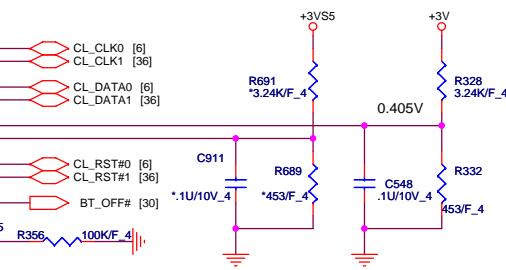
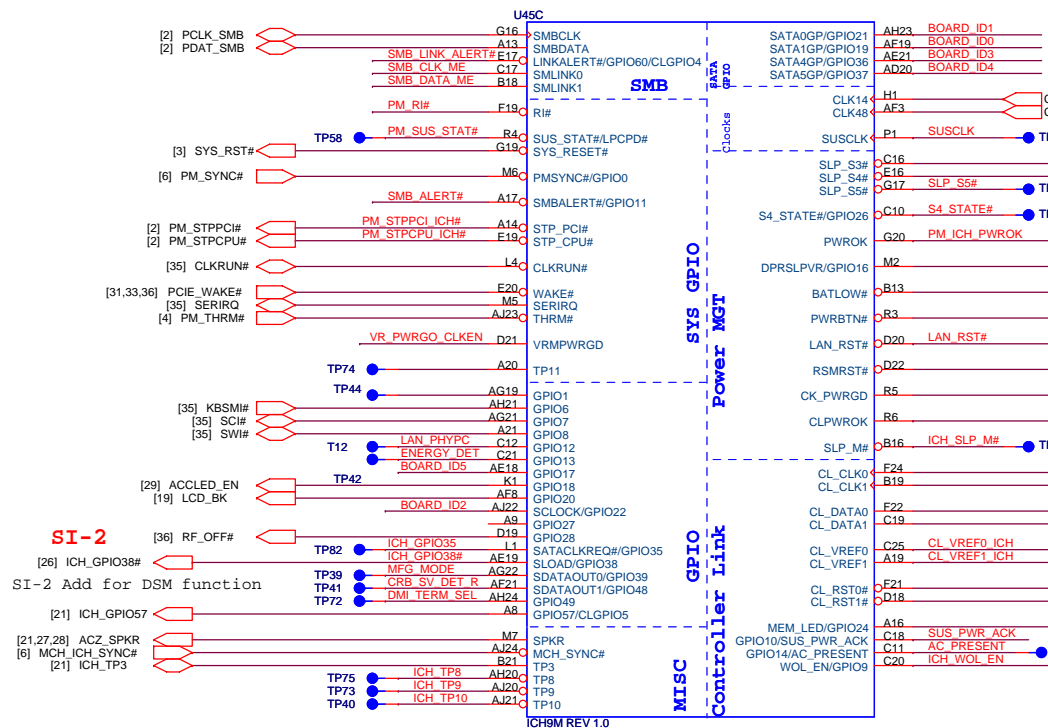
For UMA HDMI function





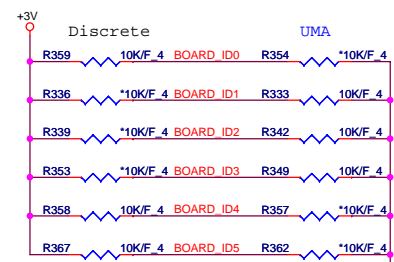
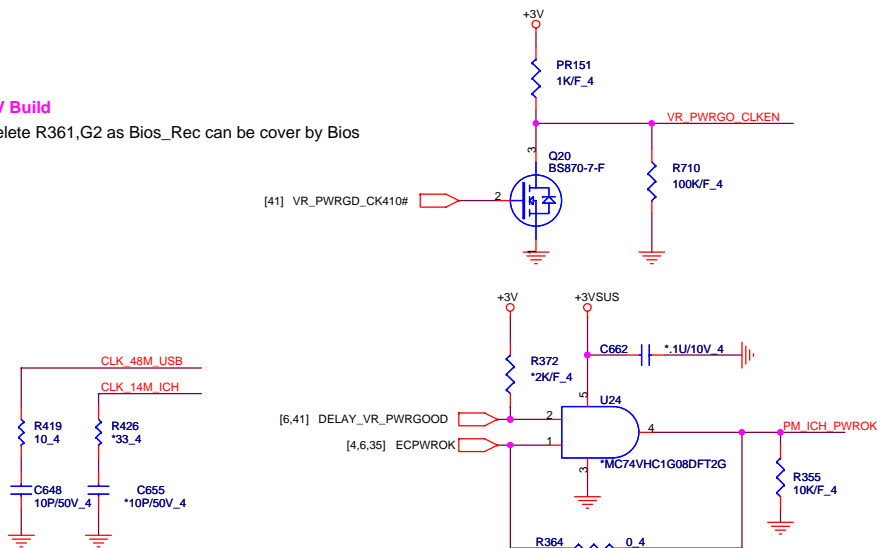
Size Custom	Document Number ICH9-M PCIE 2/4	Rev 2B
Date: Tuesday, February 26, 2008		Sheet 22 of 44

[2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,31,33,35,36,37,41,44] +1.5V
[21,22,24,33,44] +3V
[25,30,36,40,41,42,44] +3VSUS



PV Build

Delete R361,G2 as Bios_Rec can be cover by Bios

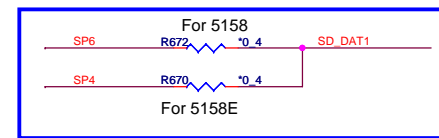
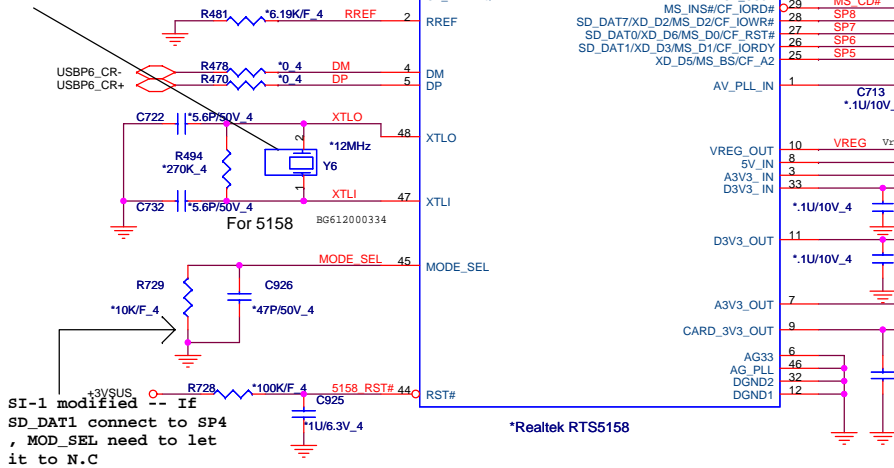




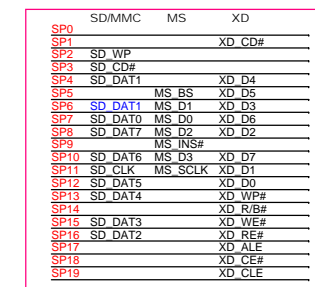
Size Custom	Document Number ICH9-M Power 4/4	Rev 1A
Date: Tuesday, February 26, 2008		Sheet 24 of 44



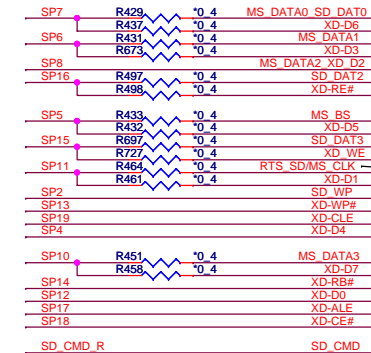
Fix Y6 layout footprint to
XTAL-5X3_2-3_8 (ME placement)



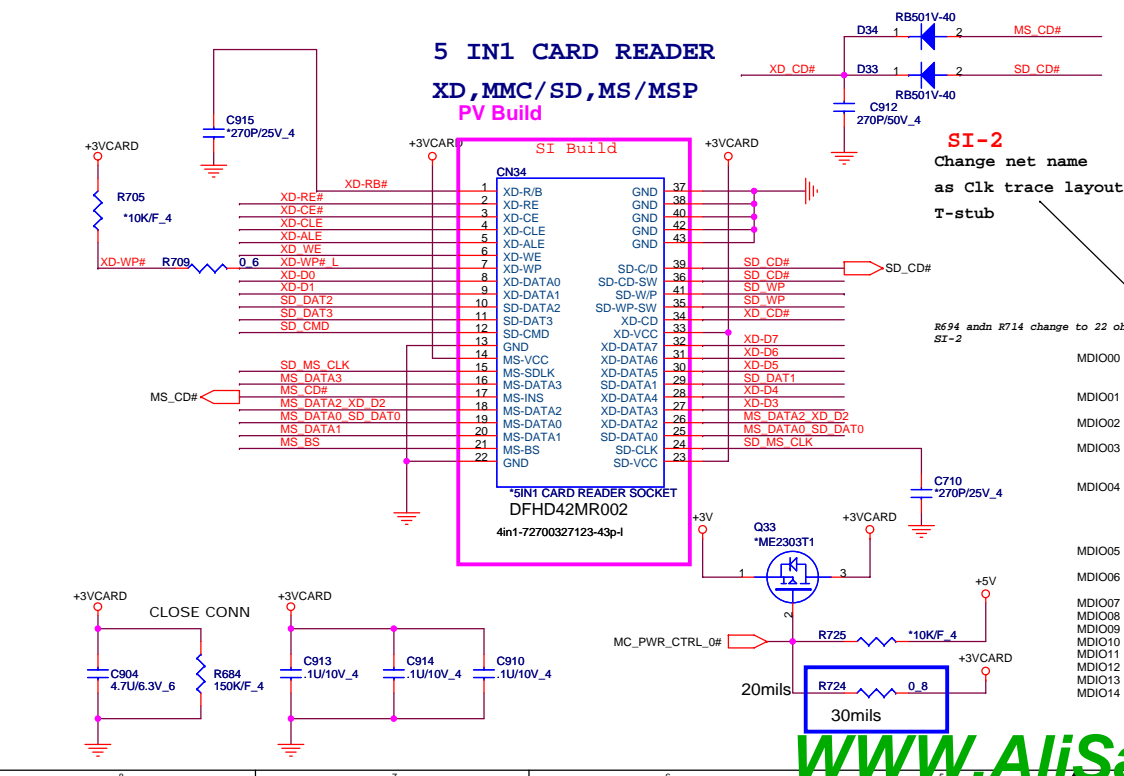
AL005158B10 -->RTS5158E
AL005158B00 -->RTS5158



For RTS5158



SI-2
Change net name
as Clk trace layout
T-stub



JMB 380 Note:

	SD/MMC	MS	XD
MDI0	SD DAT0	MS D0	XD D1
MDI1	SD DAT1	MS D1	XD D2
MDI2	SD DAT2	MS D2	XD D2
MDI3	SD DAT3	MS D3	XD D3
MDI4	SD CMD	MS BS	XD WE#
MDI5	SD CLK	MS SCLK	XD CE#
MDI6	SD WP		XD WP#
MDI7		CLE	
MDI8	SD DAT4		XD D4
MDI9	SD DAT5		XD D5
MDI10	SD DAT6		XD D6
MDI11	SD DAT7		XD D7
MDI12			XD R#
MDI13			XD B/B#
MDI14			XD ALE
CR1 LED1	SD1 LED#	MS1 LED#	XD LED#
CR1 PCTLN	SD1 PCTL#	MS1 PCTL#	XD PCTL#
CR1 CD0	SD1 CD#		XD CV#
CR1 CDT		MS1 CD#	XD CD#

SI-2
Change net name
as Clk trace layout
T-stub

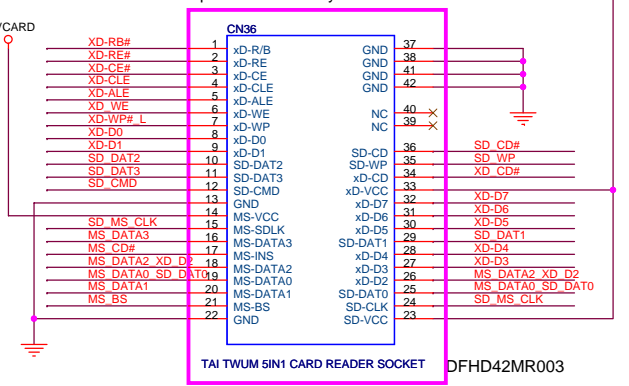
R694 andn R714 change to 22 oh
SI-2

For JMB380

R680	0.4	XD-D0
R681	0.4	XD-D1
R669	0.4	SD DAT1
R671	0.4	MS DATA1
R670	0.4	XD-D7
R687	0.4	MS DATA2 XD D2
R702	0.4	SD DAT2
R693	0.4	MS DATA3
R699	0.4	SD DAT3
R675	0.4	XD-D3
R698	0.4	SD CMD
R682	0.4	MS BS
R711	0.4	XD WE
R694	22.4	JMB SD/MS CLK
R714	0.4	XD-DCE#
R662	0.4	SD WP
R708	0.4	XD-WP#
R713	0.4	XD-CLE
R676	0.4	XD-D4
R668	0.4	XD-D5
R666	0.4	XD-D6
R663	0.4	XD-D7
R715	0.4	XD-RE#
R716	0.4	XD-RB#
R712	0.4	XD-AL#

PV Build

Update CN36 library to 7IN1-R015-B11-LM-42P-L



Close to CN34

From JMB380

From RTS5158E

New add R707,R717 for SD/MS CLK trace layout

SI-2

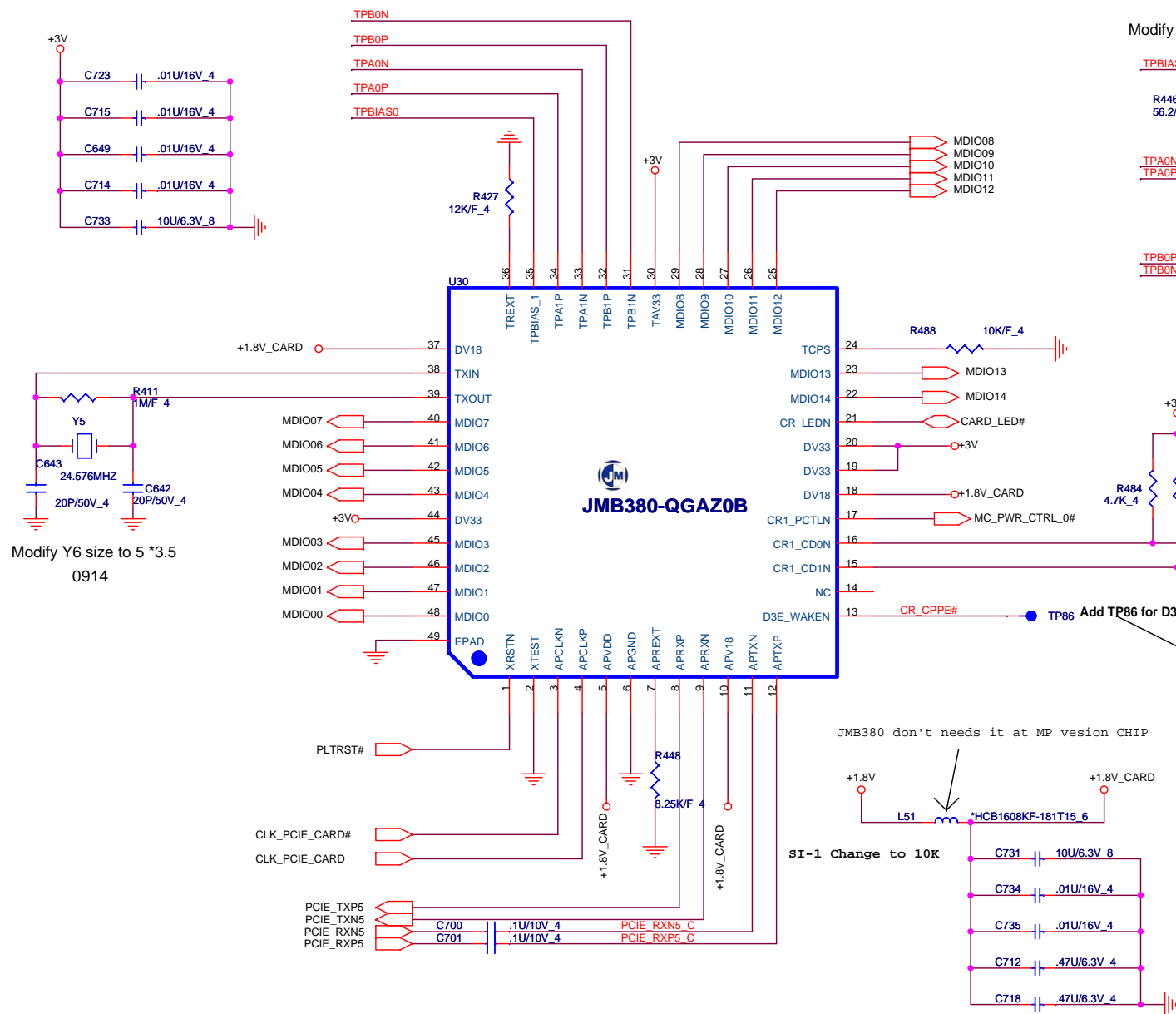
JMB SD/MS CLK R707 0.4 SD MS CLK

RTS_SD/MS_CLK R717 *0_4 SD_MS_CLK

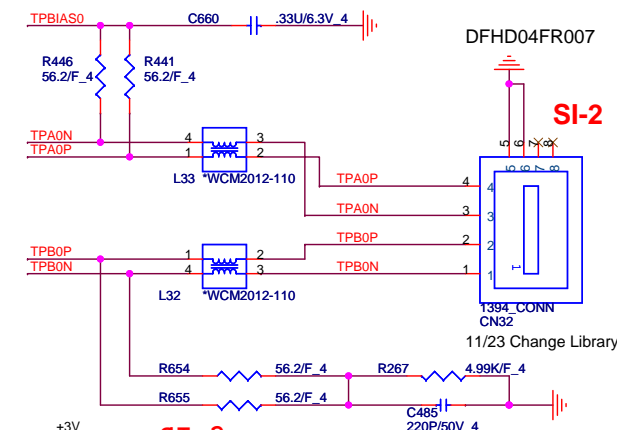


PROJECT : QT6
Quanta Computer Inc.

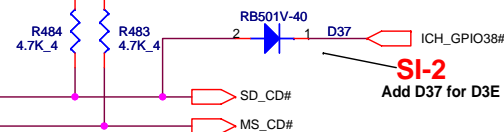
Size Custom	Document Number RTS5158 & CR SOCKET &HOLE	Rev 2B
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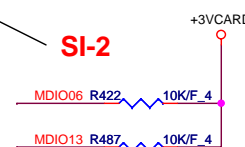
PV Build
Modify CN32 layout footprint to 1394-020115FR004S510ZL-4P-H-QT6



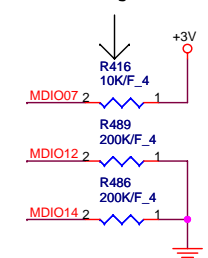
Modify CN32 layout footprint to 1394-020115FR004S510ZL-4P-H-QT6 (11/19)



SI-2

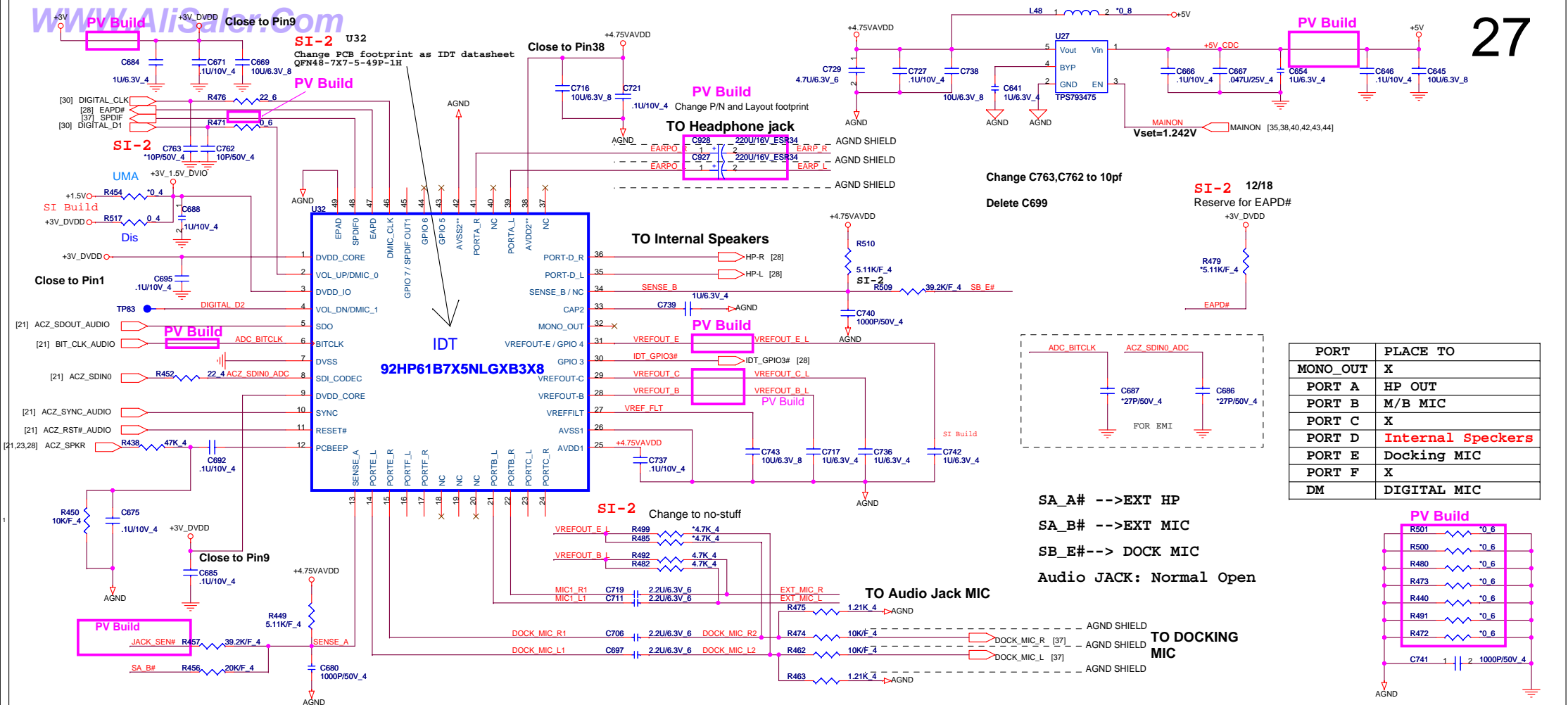


SI-1 Change to 10K



PROJECT : QT6
Quanta Computer Inc.

Size B	Document Number	Rev
	JMB380 Controller/1394	2B
Date: Tuesday, February 26, 2008	Sheet 26 of 44	

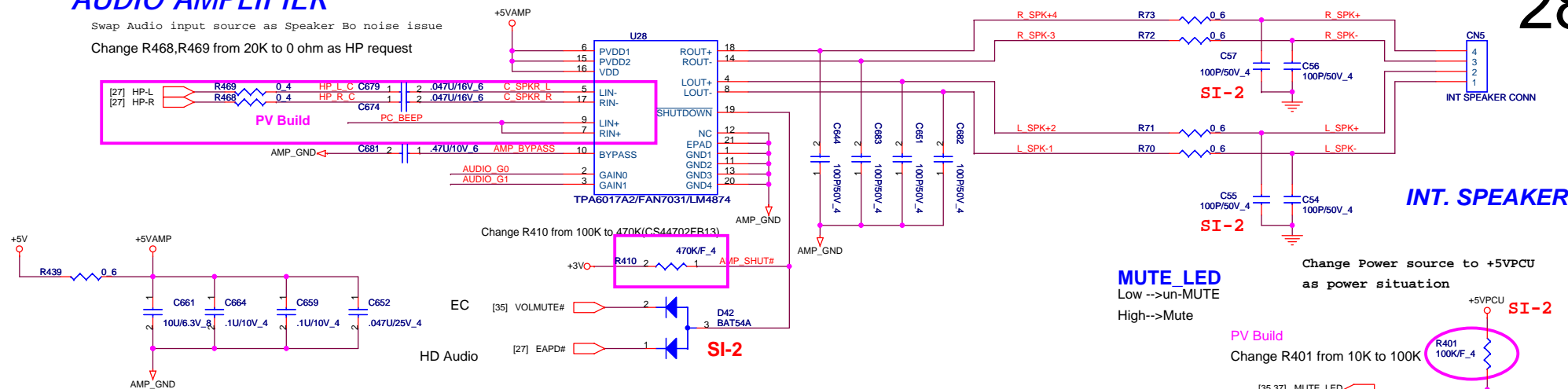


PROJECT : QT6
Quanta Computer Inc.

Size Custom	Document Number Azalia IDT92HD71B7	Rev 3A
Date: Tuesday, February 26, 2008 Sheet 27 of 44		

Swap Audio input source as Speaker Bo noise issue

Change R468,R469 from 20K to 0 ohm as HP request

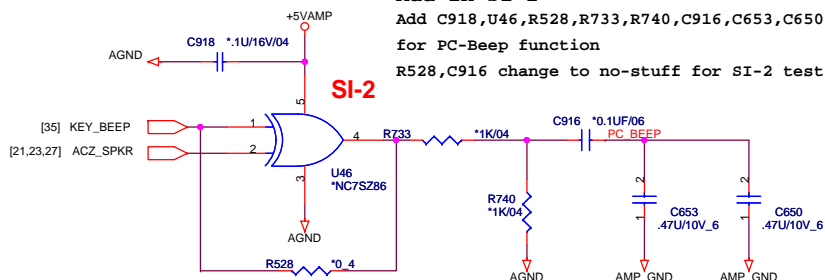


Add in SI-2

Add C918,U46,R528,R733,R740,C916,C653,C650

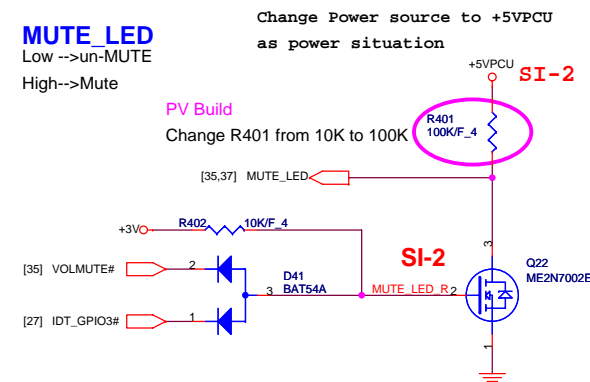
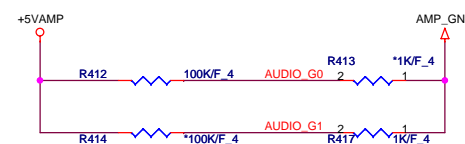
for PC-Beep function

R528,C916 change to no-stuff for SI-2 test -->12/6

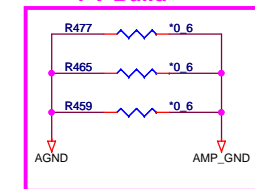


6017A2 Gain Table

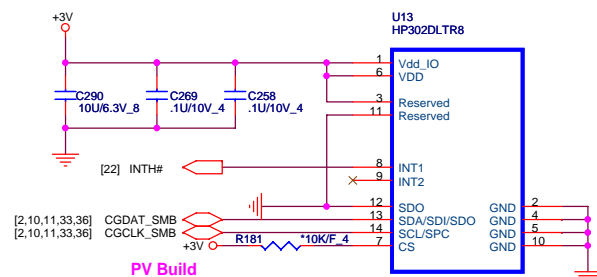
GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K



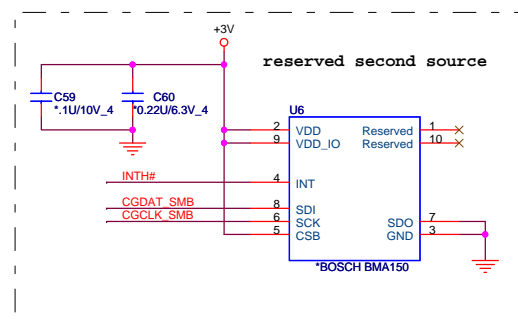
PV Build



Accelerometer Sensor

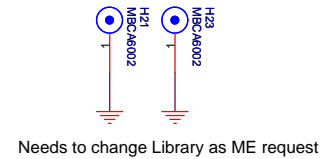
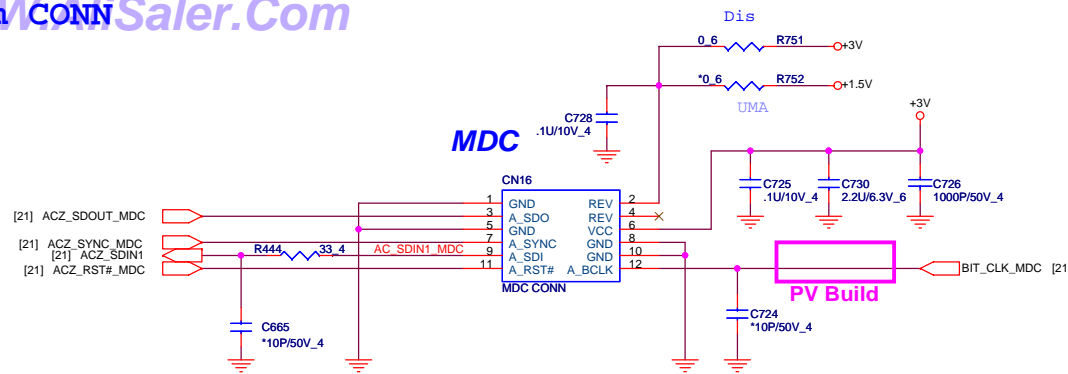


Change R181 to no stuff as internal pull high

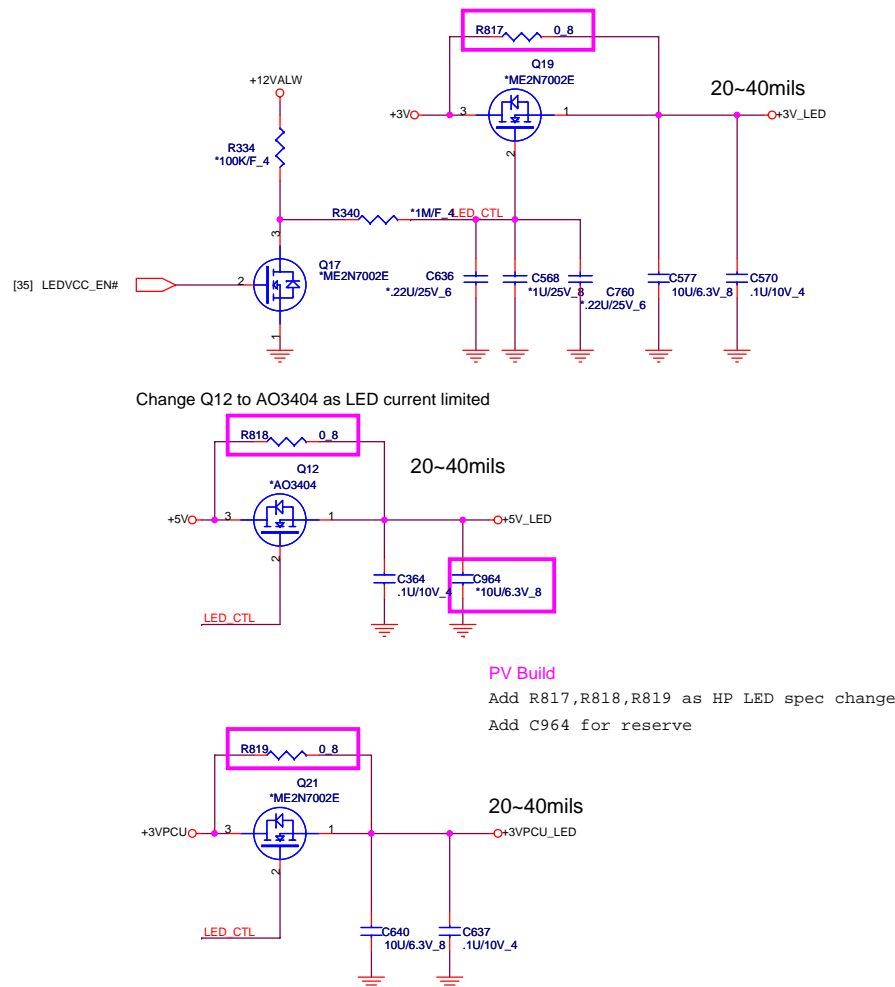


Pin 12: Low 38hex

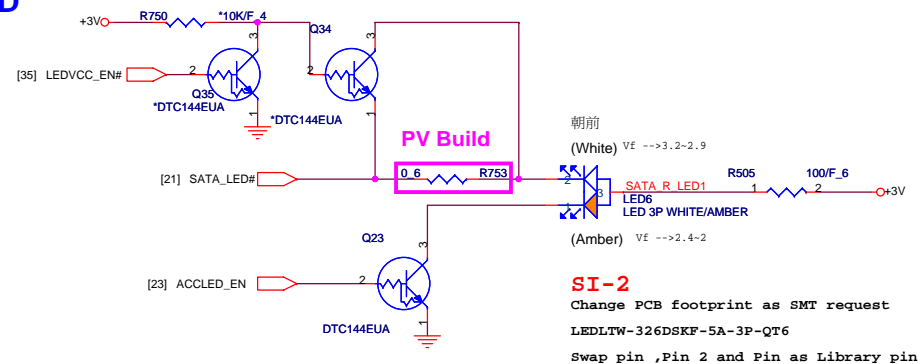
Pin 12: unconnected/floating 3Ahex



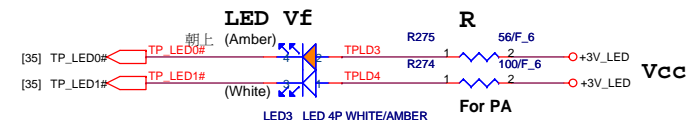
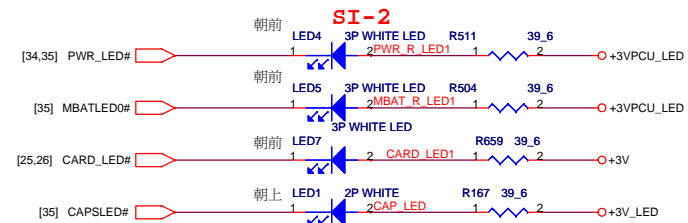
LED PWR CONTROL



LED



Modify LED4,LED5,LED7 layout footprint to led1-s110kgct-3p-qt6 (11/19)

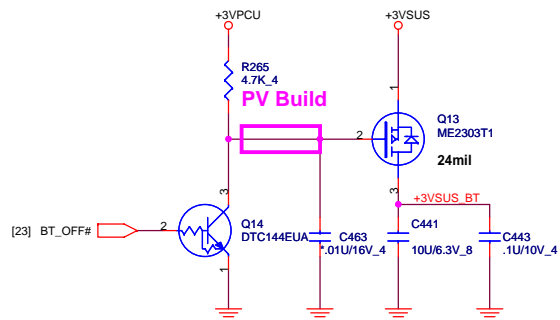


$$I = \frac{V_{cc} - V_f}{R}$$



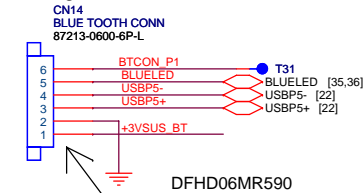
PROJECT : QT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MDC/LED	3A
Date: Tuesday, February 26, 2008	Sheet 29 of 44	



PV Build

Change CN14 P/N to DFHD06MR590



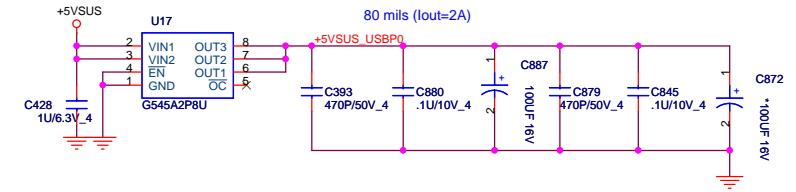
SI-2

CN14 and CN9 87213-0600-6P-L

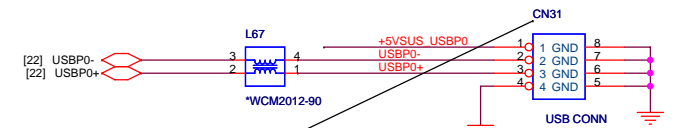
Change footprint as ME request (pitch 1.25mm to 1.0mm)

LEFT SIDE USBX1 and E-SATA/USB COMBO

30



USB 0



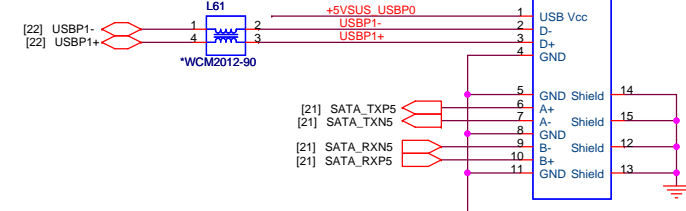
SI-2

CN30, CN31

USB-020173MR004S51BZR-4P-R-H

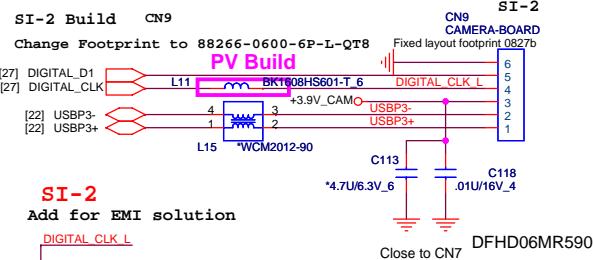
Change Connector layout type from SMD PAD to Dip as SMT request

USB & ESATA

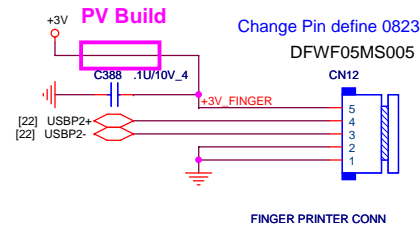


USB-C-2006102-11P-H-QT6

USB CAMERA /DIGITAL MIC CONNECT



USB fingerprint CON

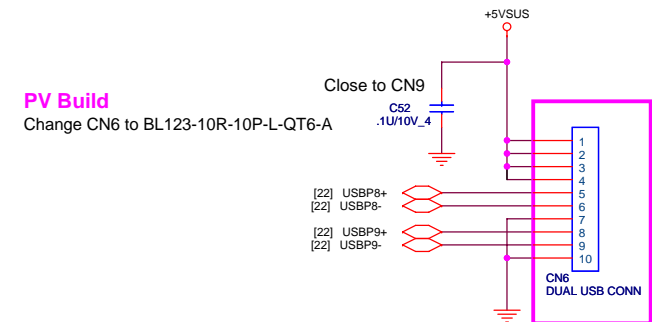


PV Build

Change CN12 to BL123-05R-5P-L-QT6-A

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

RIGHT SIDE USBX2

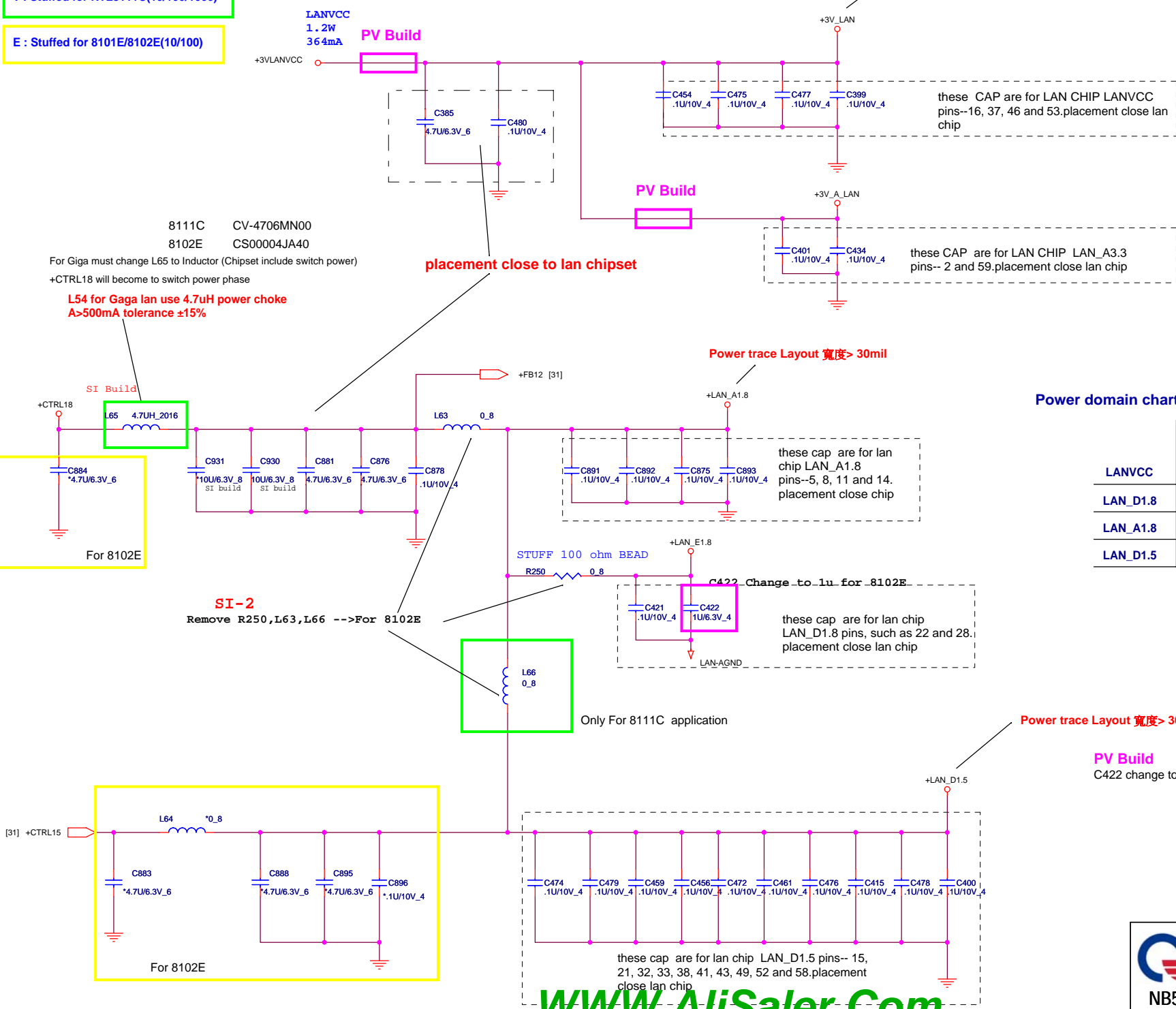


PROJECT : QT6
Quanta Computer Inc.

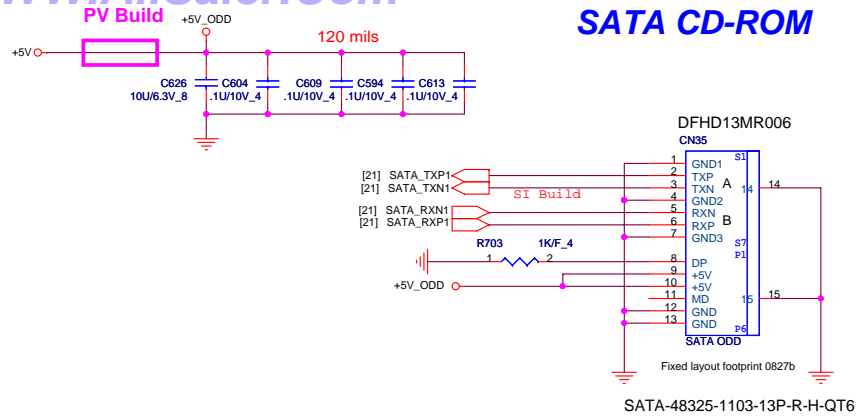
Size	Document Number	Rev
Custom	BT/WC/FT/TS/ESATA/USB	3A
Date: Tuesday, February 26, 2008	Sheet 30 of 44	

T : Stuffed for RTL8111C(10/100/1000)

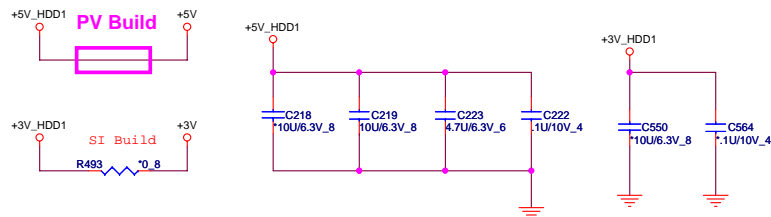
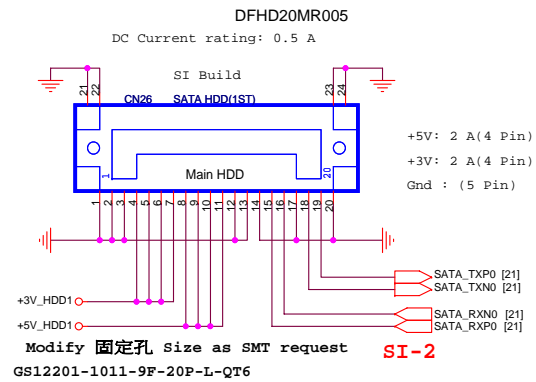
E : Stuffed for 8101E/8102E(10/100)



SATA CD-ROM

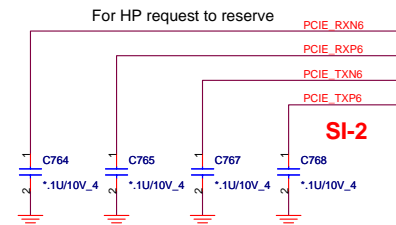
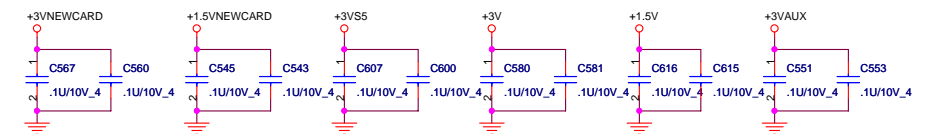
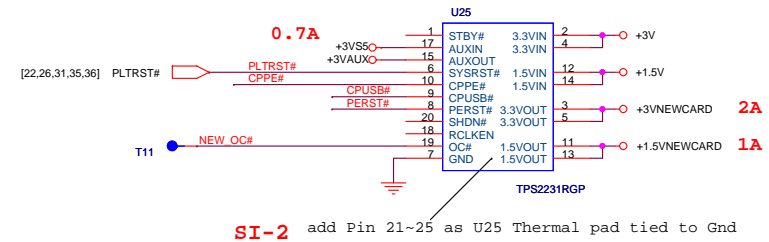
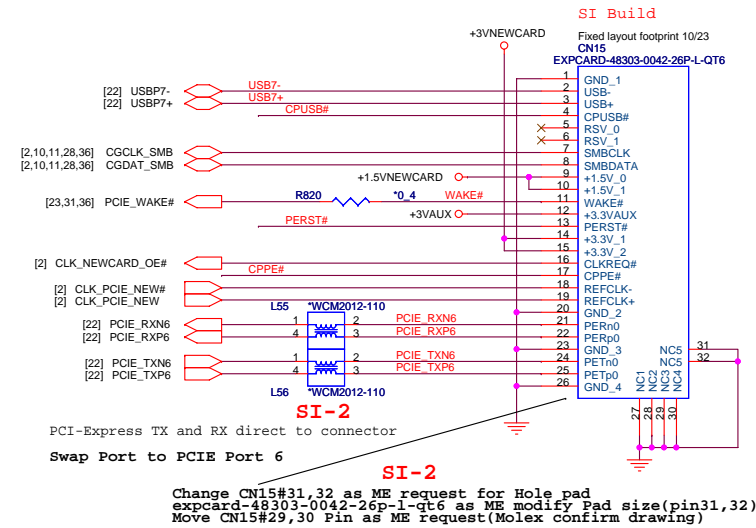


SATA HDD CONNECTOR

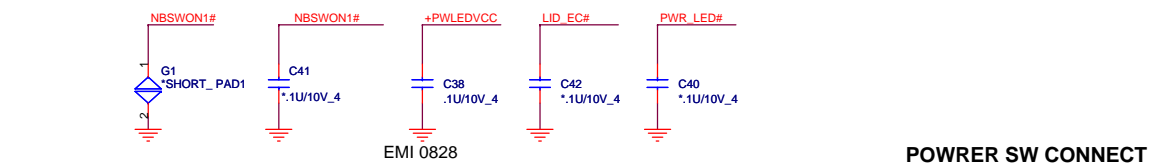
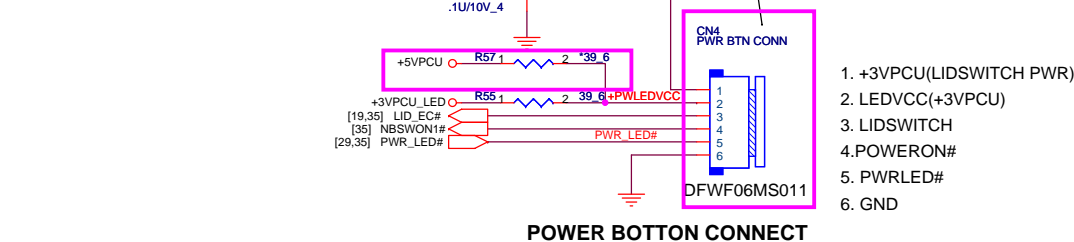
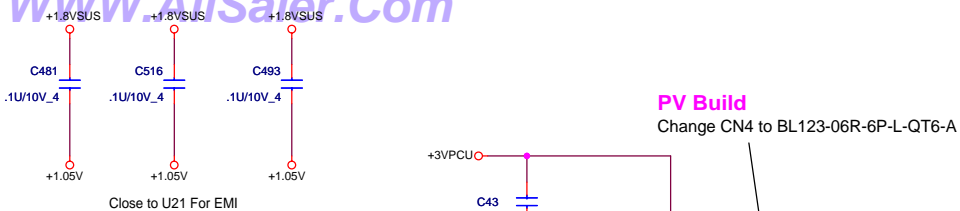


NEWCARD

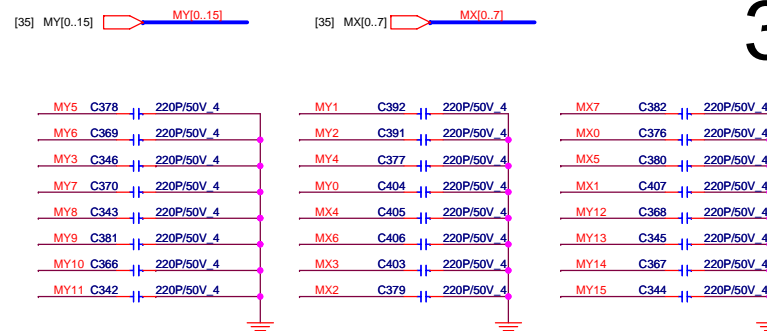
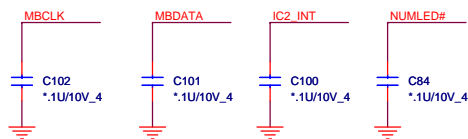
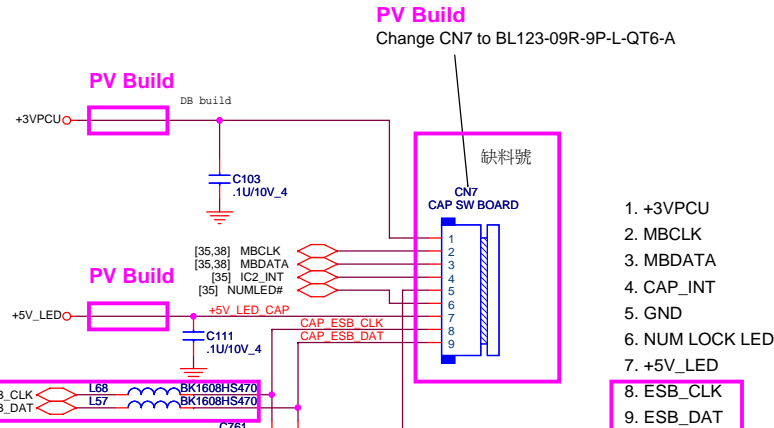
NEWCARD (PCIEXPRESS*1 + USB*1)



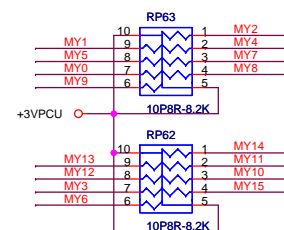
NB5	PROJECT : QT6 Quanta Computer Inc.		
	Size Custom	Document Number ODD/HDD/NEW CARD	Rev 2B
Date: Tuesday, February 26, 2008 1 Sheet 33 of 44			



CAP SW CONNECT



KEYBOARD PULL-UP

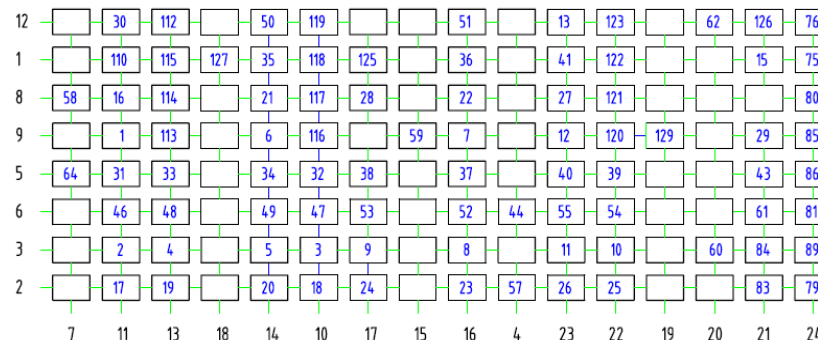
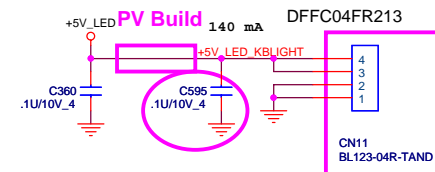
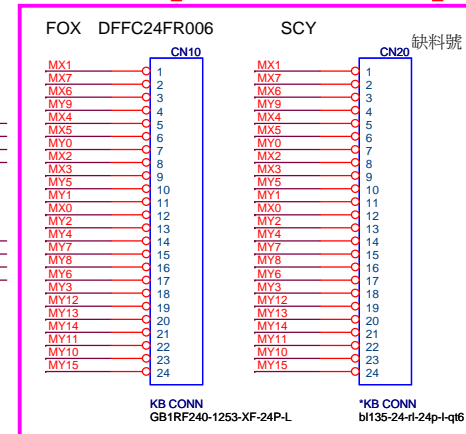


PV Build

Add C595 and close to CN11

Change CN11 to BL123-04R-4P-L-QT6-A

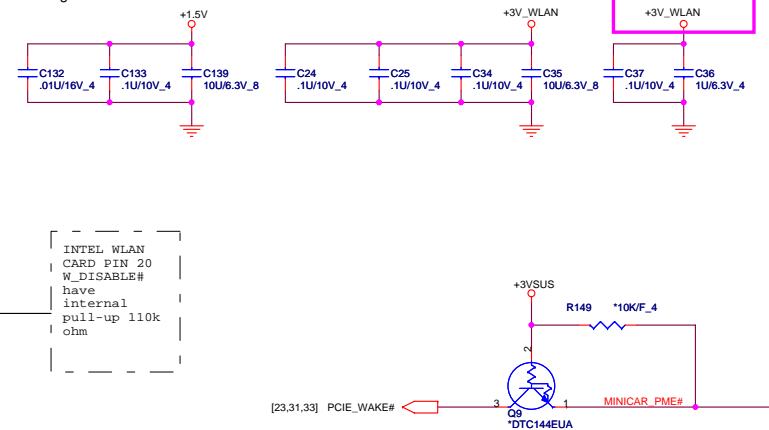
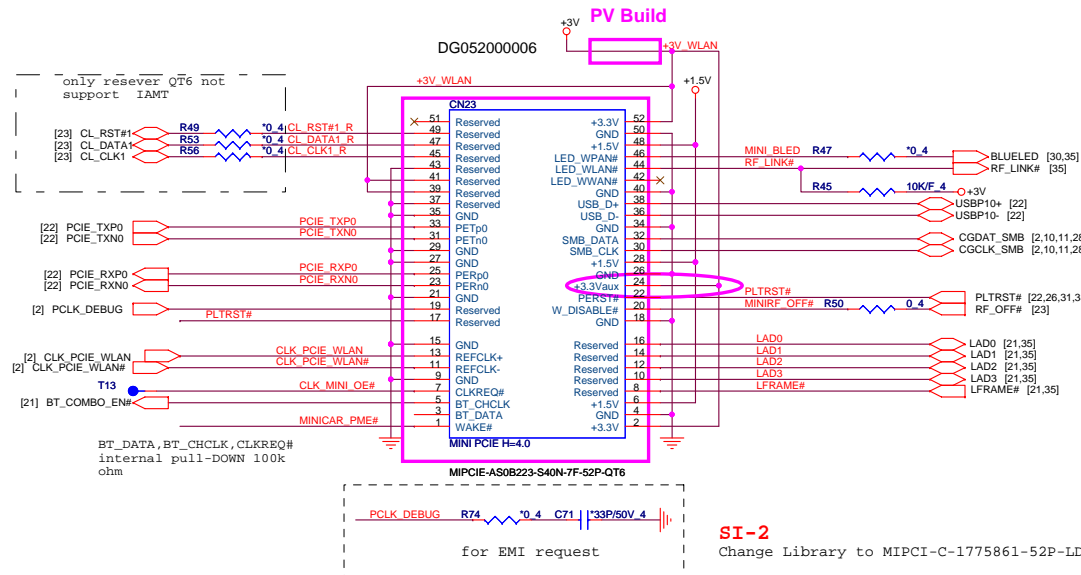
Change CN10 to GB1RF240-1253-XF-24P-L as Foxconn drawing



PROJECT : QT6
Quanta Computer Inc.

Size Custom	Document Number KB/CAP/POWER CONN	Rev 21
Date: Tuesday, February 26, 2008 Sheet 34 of 44		

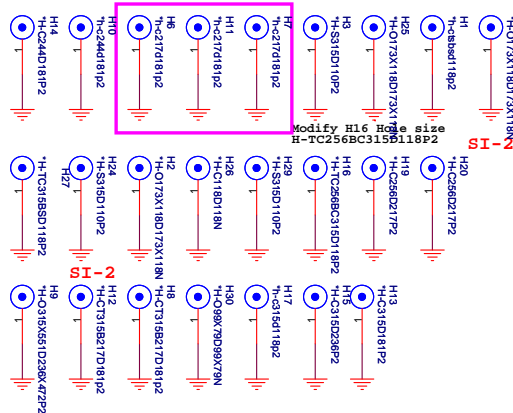




SI-2
Change Library to MIPCI-C-1775861-52P-LDV-QT6 12/11

M/B Screw Hole

SI-2,h-e276x315d118p2



SI-2 New add as ME request

RF PAD ME PAD

Routed spring

PV Build
Delete PAD14

RAD15



*MDC_SPRING

PAD16

*MDC_SPRING

EMI PA

PAD2 PA

*EMIPAD *EM



PA

*EM

1

100

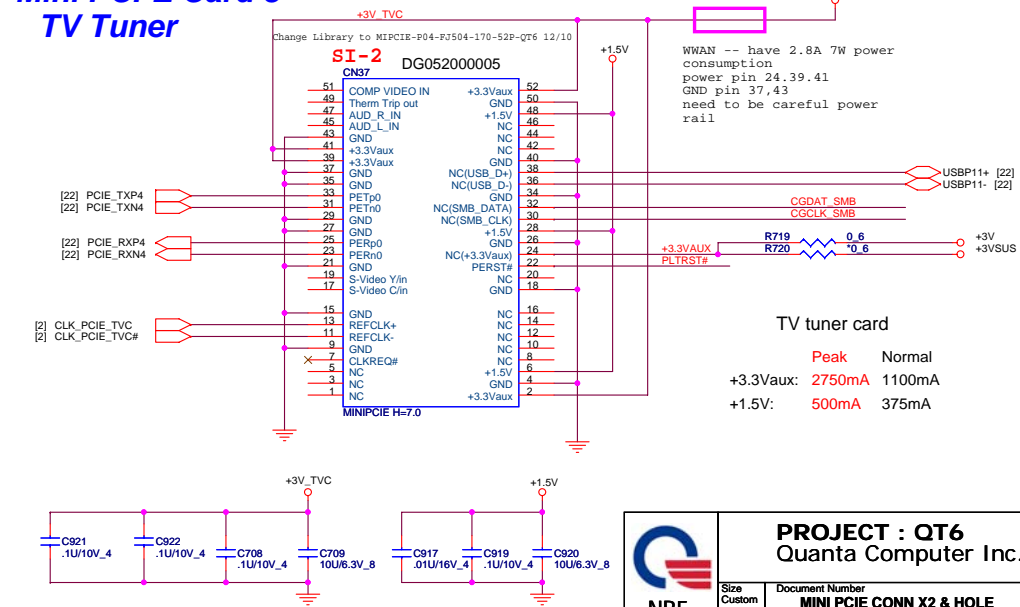
□ □ □ □

WZ

///

Mini PCI-E Card 3 TV Tuner

PV Build



```
WWAN -- have 2.8A 7W power
consumption
power pin 24.39.41
GND pin 37,43
need to be careful power
rail
```

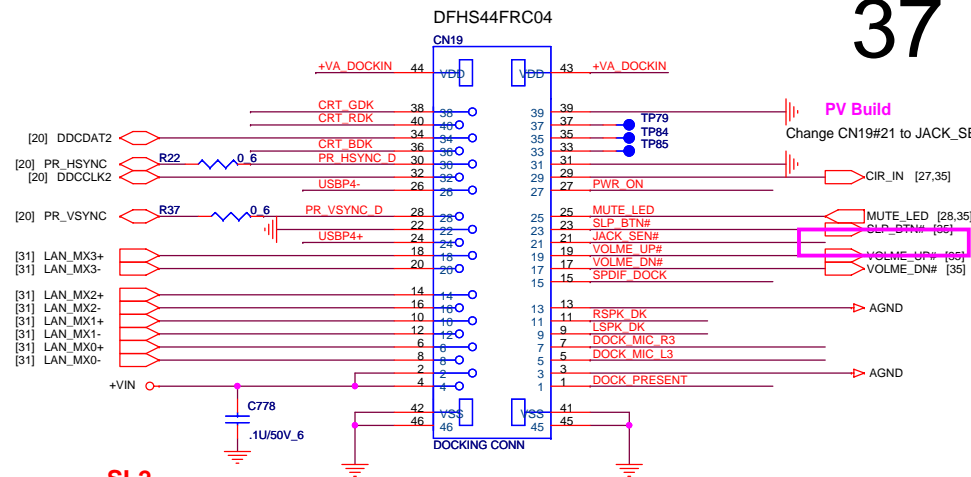
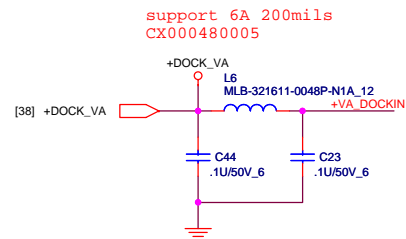
TV tuner card

	Peak	Normal
+3.3Vaux:	2750mA	1100mA
+1.5V:	500mA	375mA

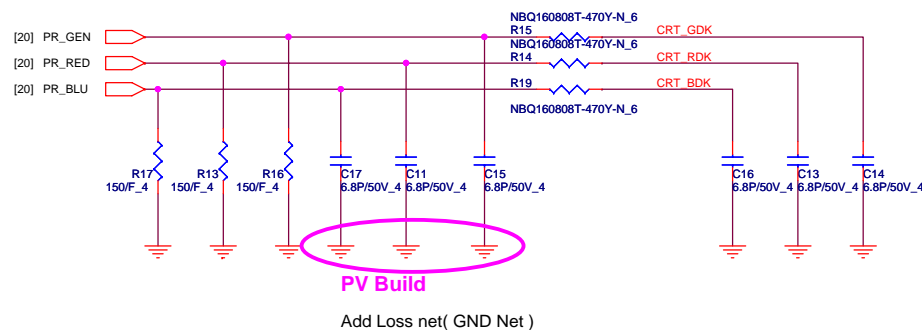
V Build	
1/25	Change H1 to h-ctsbdsd118p2 Add PAD17 (Emi157x79) Add PAD18 (Emi157x79) Add PAD19 (Emi236x59)
1/29	Delete H4,H5 and modify battery connector
1/31	Change H6,H7,H11 to h-c217d181p2 as ME drawing update

PROJECT : QT6
Quanta Computer Inc.

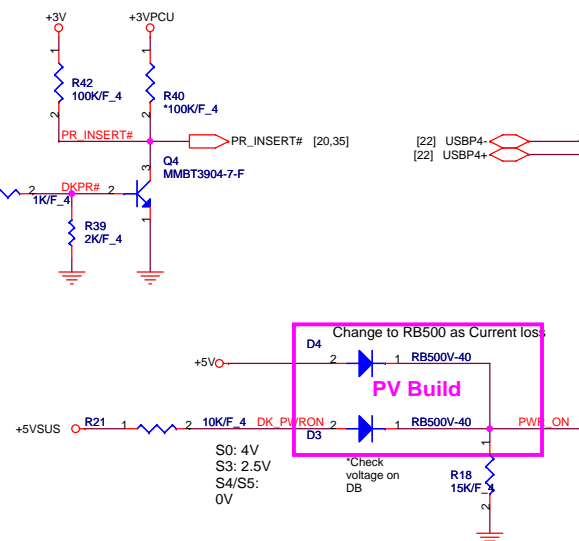
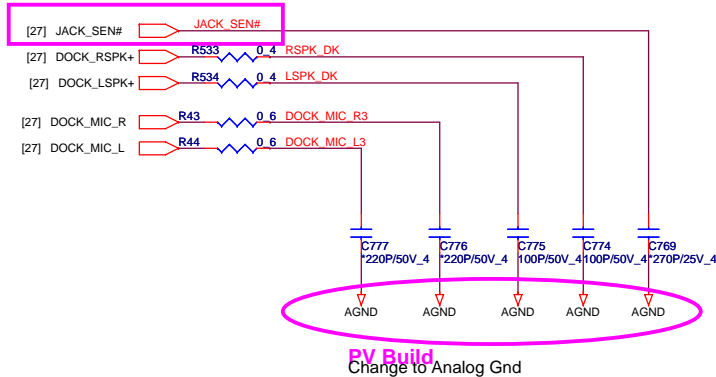
Size Custom	Document Number MINI PCIE CONN X2 & HOLE	Rev 2B
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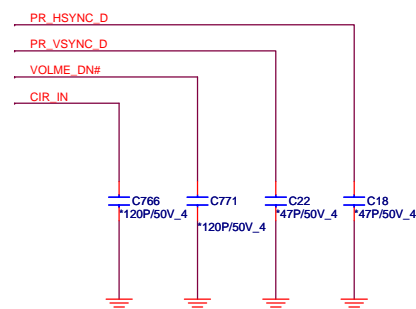
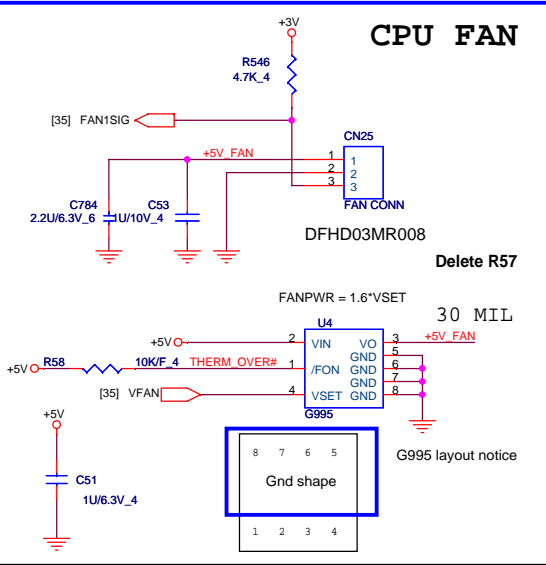
SI-2
R13,R16,R17 Change to install

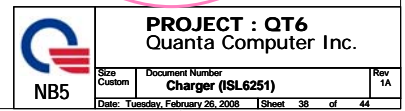


PV Build



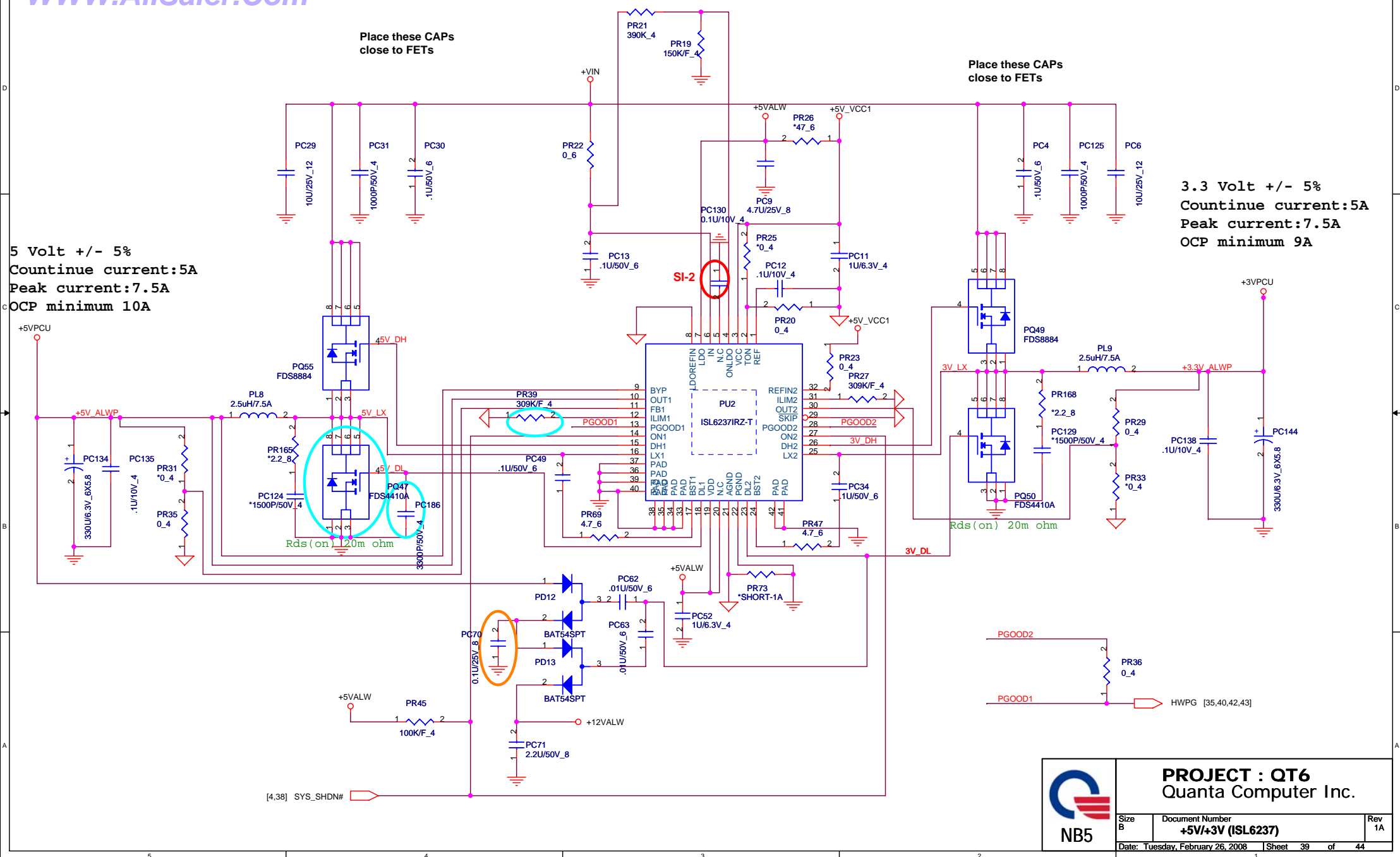
CPU FAN



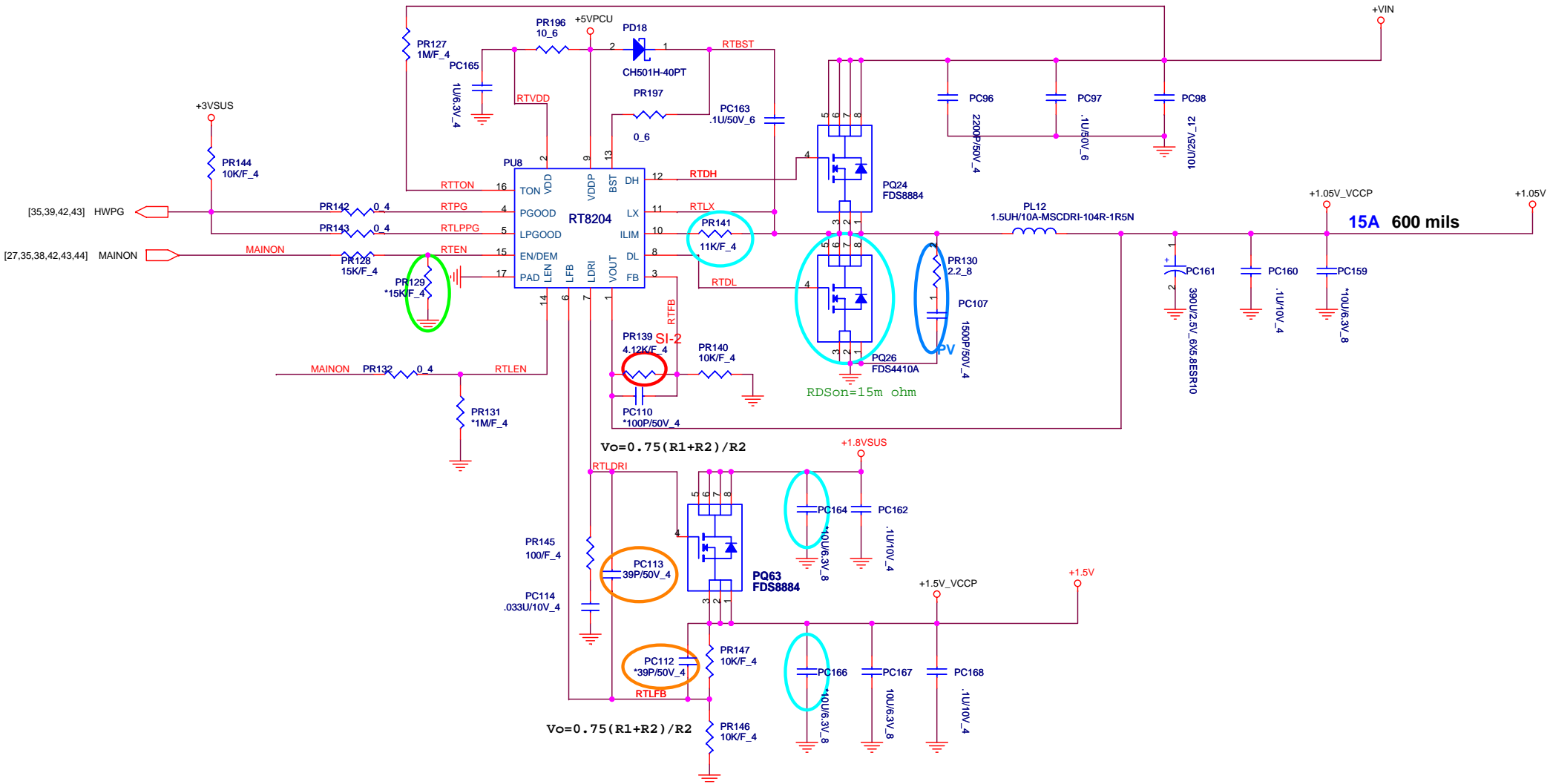



5 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 9A



+1.05Volt +/- 5%
Countinue current:7.5A
Peak current:10A
OCp minimum 15A

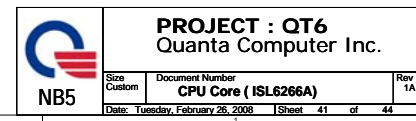




PROJECT : QT6

Quanta Computer Inc.

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```
+1.1Volt +/- 5%
Countinue current:17.54A
Peak current:22.8A
OCP minimum 23A
```

